SPI/QPI PSRAM

Specifications

- **Single Supply Voltage**
  - V_{DD}=1.62 to 1.98V
- **Interface**: SPI/QPI with SDR mode
- **Performance**: Clock rate up to 144MHz
- **Organization**: 16Mb, 2M x 8bits
- **Addressable Bit Range**: A[20:0]
- **Page Size**: 512 bytes
- **Refresh**: Self-managed
- **Operating Temperature Range**
  - Tc= -40°C to +85°C (standard range)
  - Tc= -40°C to +105°C (extended range)
- **Maximum Standby Current**
  - 150µA @ 105°C
  - 100µA @ 85°C
  - 25µA @ 25°C

Features

- **Output Driver LVCMOS** with programmable drive strengths of 50, 100 and 200Ω
- **Dedicated Wrapped Burst** read and write commands
- **Bursts Wrapped** as long as tCEM is met.
- **Register Configurable Wrap Lengths** of 16, 32, 64 and 512
- **Toggle Command** to switch between configurable wrap length and 32 bytes wrap
- **Software Reset**

Table of Contents

2 Introduction

This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 I/O pins and operates in SPI(serial peripheral interface) or QPI (quad peripheral interface) mode with frequencies up to 144 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

3 Package Information

The APS1604M-SQ is available in standard package including 8-lead SOP-8L(150) and advanced package including 8-lead , USON-8L 3x2mm.

● **Package Types (not to scale)**

SOP / USON

(SN, ZR)

/CE	1		8	VDD
SO/SIO[1]	2		7	SIO[3]
SIO[2]	3		6	SCLK
VSS	4		5	SI/SIO[0]
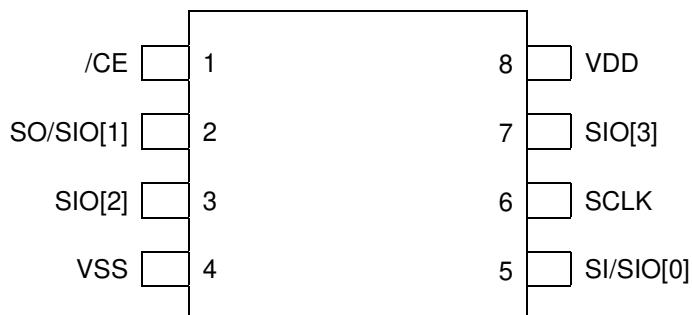
4　Package Outline Drawing

4.1　SOP-8L(150), package code SN
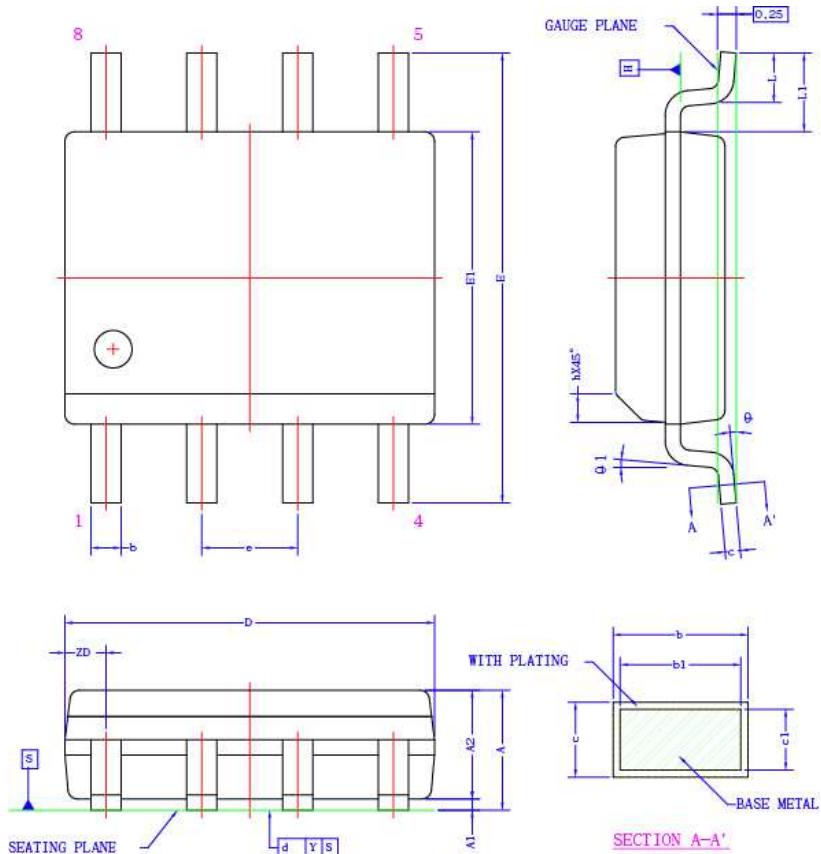
| SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2	1.35	1.45	1.55	53	57	61
b	0.31	–	0.51	12	–	20
b1	0.28	0.40	0.48	11	16	19
c	0.17	–	0.25	7	–	10
c1	0.17	0.20	0.23	7	8	9
D	4.80	4.90	5.00	189	193	197
E	6.00 BSC			236 BSC		
E1	3.80	3.90	4.00	150	154	157
e	1.27 BSC			50 BSC		
L	0.40	0.66	1.27	16	26	50
L1	1.05 REF			41 REF		
ZD	0.55 REF			22 REF		
h	0.25	0.38	0.50	10	15	20
Y	–	–	0.10	–	–	4
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–

NOTE :

1. REFER TO JEDEC STD: MS-012 AA.

2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
DIMENSION "E1" DOES NOT INCLUDE INTERLEAD MOLD FLASH OR PROTRUSION. INTERLEAD MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
'D' AND 'E1' DIMENSIONS ARE DETERMIND AT DATUM H .

3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

4.2 USON-8L 3x2mm, package code ZR

Pin1
0.15x45°

8 | 1

E1

e

D1

DETAIL B

Bottom View

0.15 C

D

A

B

Pin1 Index

E

0.15 C

Top View

DETAIL A

0.10 C

C

SEATING PLANE

0.08 C

Side View

A

A1

L1
L2
L

DETAIL A

b

0.10 Ⓜ C A B
0.05 Ⓜ C

DETAIL B

Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	---	0.05
D	2.90	3.00	3.10
D1	0.10	0.20	0.30
E	1.90	2.00	2.10
E1	1.50	1.60	1.70
L	0.40	0.45	0.50
L1	---	0.40	---
L2	---	0.05	---
b	0.20	0.25	0.30
e	0.50 BSC		
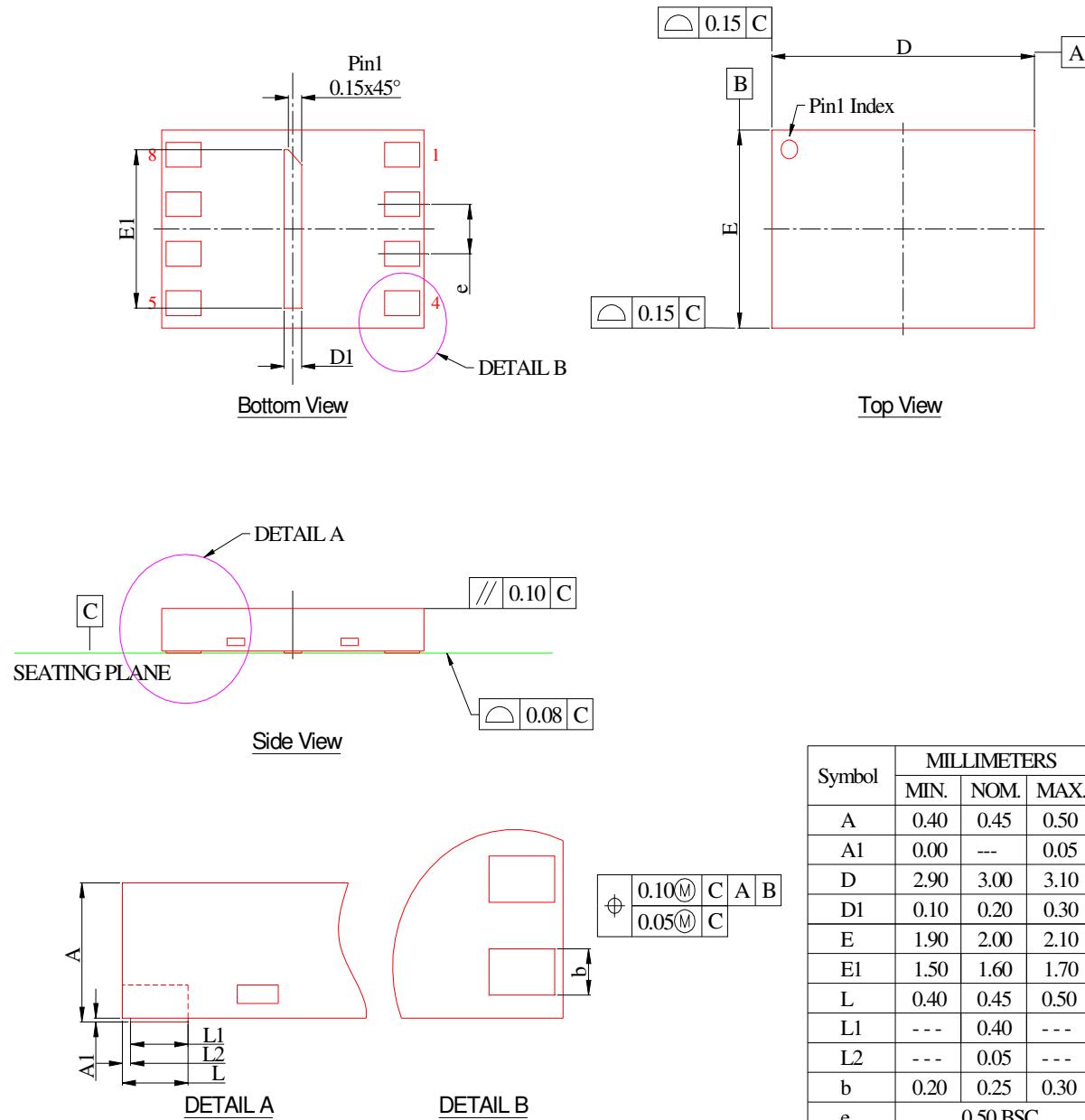
NOTE:
1. Scale 1:4
2. ALL DIMENSIONS AND TOLERANCES TAKE REFERANCE TO JEDEC MO-229
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN
   0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL
   RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE
   MEASURED IN THAT RADIUS AREA.

5   Ordering Information

Table 1: Ordering Information

Part Number	Temperature	Max Frequency	Note
APS1604M-SQ-ZR	-25°C to +85°C	144 MHz	USON-8
APS1604M-SQ-SN	-40°C to +85°C	144 MHz	SOP-8
APS1604M-SQX-SN	-40°C to +105°C	144 MHz	SOP-8

```
 A   P   S   16  04   M            SQ

            128                              X
            256
            32
            64
```

S: Sync

Die Gen.

IO Config.
16: x16
08: x8
04: x1/x4

PSRAM

Density
256: 256M
128: 128M
64: 64M
32: 32M
16: 16M

AP Memory

VCC
Blank: 1.8V
3: 3V

Interface
SQ : Serial x1/x4 SDR

Die Option
Blank: non-RBX
R: RBX

Temperature grade
Blank: default option
X: extended temp.

Package Type
Blank: KGD
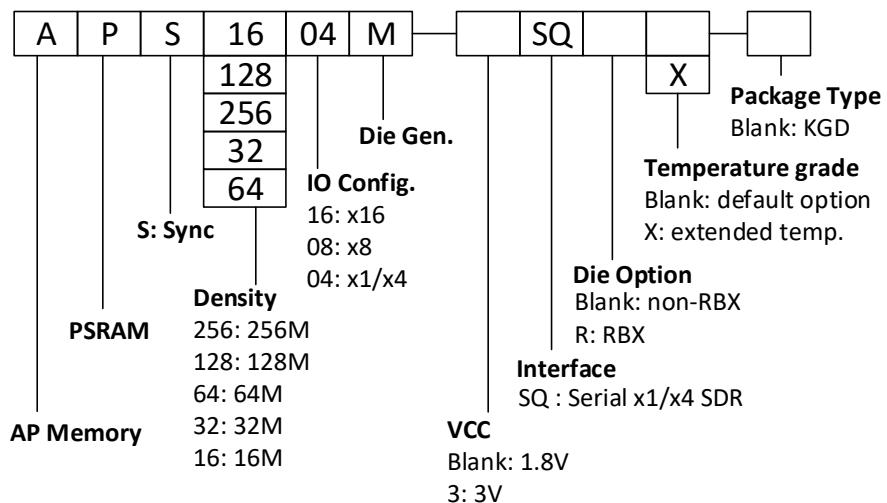
6   Signal Table

All signals are listed in Table 2.

Table 2: Signals Table

Symbol	Type	SPI Mode Function		QPI Mode Function	Comments
VDD	Power	Core supply 1.8V			
VSS	Ground	Core supply ground			
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state			
CLK	Input	Clock Signal			
SI/SIO[0]	IO	Serial Input	IO[0]*	IO[0]	
SO/SIO[1]	IO	Serial Output	IO[1]*	IO[1]	
SIO[2]	IO	--	IO[2]*	IO[2]	
SIO[3]	IO	--	IO[3]*	IO[3]	

Note *: SPI Quad mode

7   Block Diagram
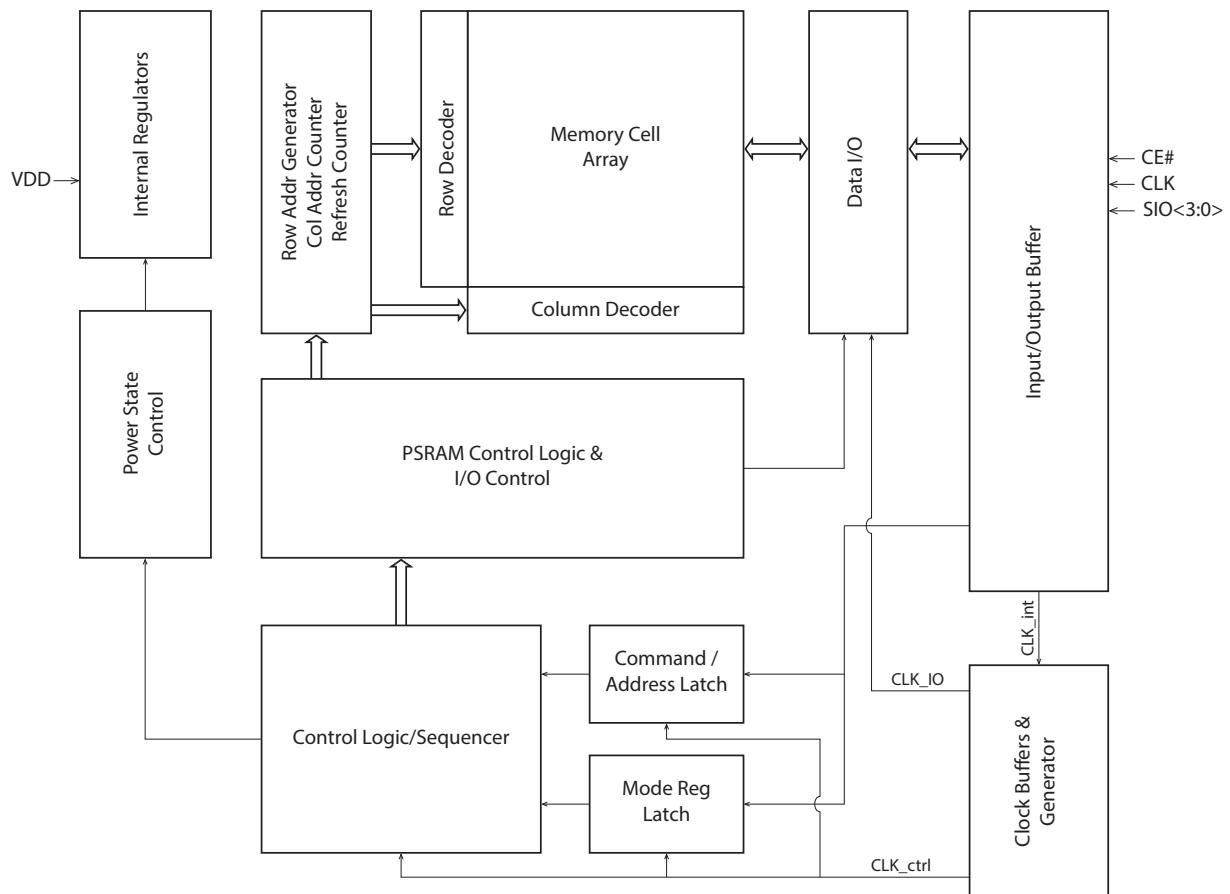
8   Power-Up Initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{DD} reaches a stable level at or above minimum V_{DD}, the device will require 150μs and user-issued RESET Operation (see section 17) to complete its self-initialization process. From the beginning of power ramp to the end of the 150μs period, CLK should remain LOW, CE# should remain HIGH (track V_{DD} within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the 150μs period the device is ready for normal operation.
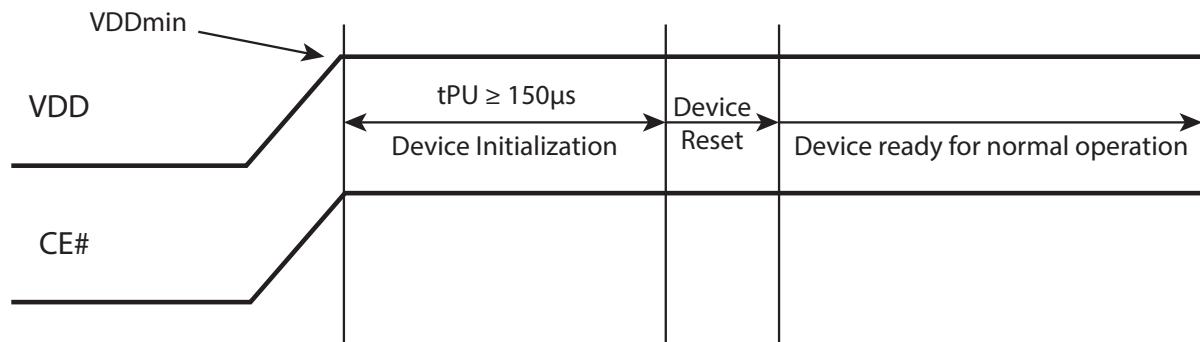
Figure 1. Power-Up Initialization Timing

9   Interface Description

9.1   Address Space

SPI/QPI PSRAM device is byte-addressable. 16M device is addressed with A[20:0].

9.2   Page Length

Read and write operations are default wrap with a page size of 512 bytes.

9.3   Drive Strength

The device powers up in 50Ω.

9.4   Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

10 Mode Register Definition

Table 3: Mode Register Table

MR No.	MA[3:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h0	R/W	rsvd.	Wrap		rsvd.			DQ Zout	

Table 4: Wrap Codes   MR0[6:5]

Wrap Burst Settings	
MR0[6:5]	**Wrapped Length**
00	16
01	32
10	64
11 (default)	512 (page size)

Table 5: DQ Output Drive Strength Codes   MR0[1:0]

DQ Output Drive Strength	
MR0[1:0]	**Impedance**
00(default)	50Ω
01	100Ω
10	200Ω
others	reserved

11 Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods. All Read/Write commends are operated in a wrap manner.

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	Max Freq.	Cmd	Addr	Wait Cycle	DIO	Max Freq.
Read	'h03	S	S	0	S	33	N/A				
Fast Read	'h0B	S	S	8	S	144	Q	Q	4	Q	66
Fast Read Quad	'hEB	S	Q	6	Q	144	Q	Q	6	Q	144
Write	'h02	S	S	0	S	144	Q	Q	0	Q	144
Quad Write	'h38	S	Q	0	Q	144	same as 'h02				
Wrapped Read	h8B	S	S	8	S	144	Q	Q	6	Q	144
Wrapped Write	h82	S	S	0	S	144	Q	Q	0	Q	144
Mode Register Read	hB5	S	S	8	S	144	Q	Q	6	Q	144
Mode Register Write	hB1	S	S	0	S	144	Q	Q	0	Q	144
Enter Quad Mode	'h35	S	-	-	-	144	N/A				
Exit Quad Mode	'hF5	N/A					Q	-	-	-	144
Reset Enable	'h66	S	-	-	-	144	Q	-	-	-	144
Reset	'h99	S	-	-	-	144	Q	-	-	-	144
Burst Length Toggle	'hC0	S	-	-	-	144	Q	-	-	-	144
Read ID	'h9F	S	S	0	S	33	N/A				
Remark: S = Serial IO, Q = Quad IO											

11.1 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.
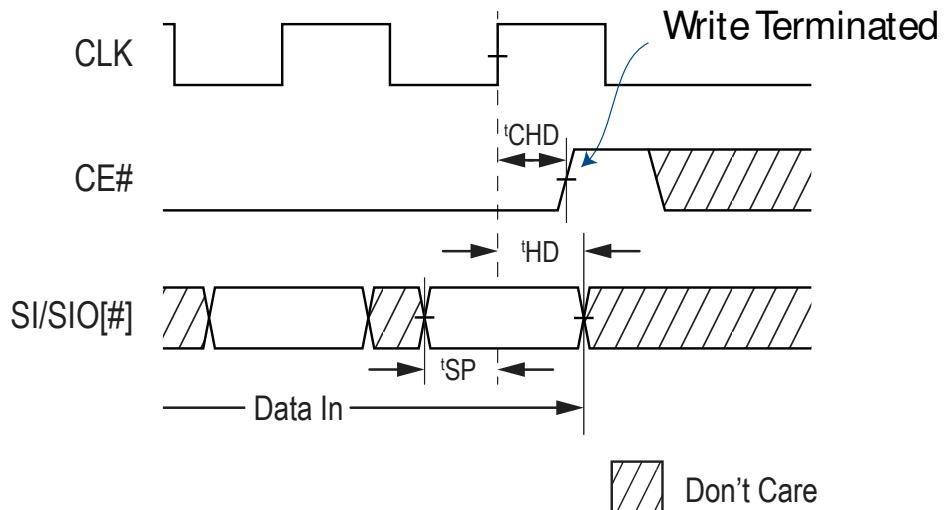

Figure 2: Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time ($^tCHD > {}^tACLK + {}^tCLK$) for a sufficient data window.
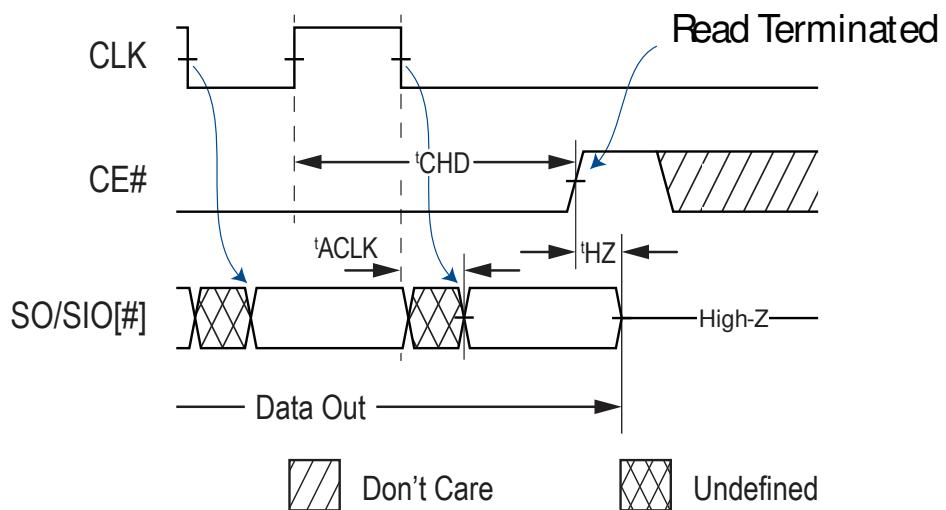
Figure 3: Read Command Termination

12 Mode Register Operations

12.1 SPI MR Read Operation

For all reads, MR data will be available ^{t}ACLK after the falling edge of CLK.
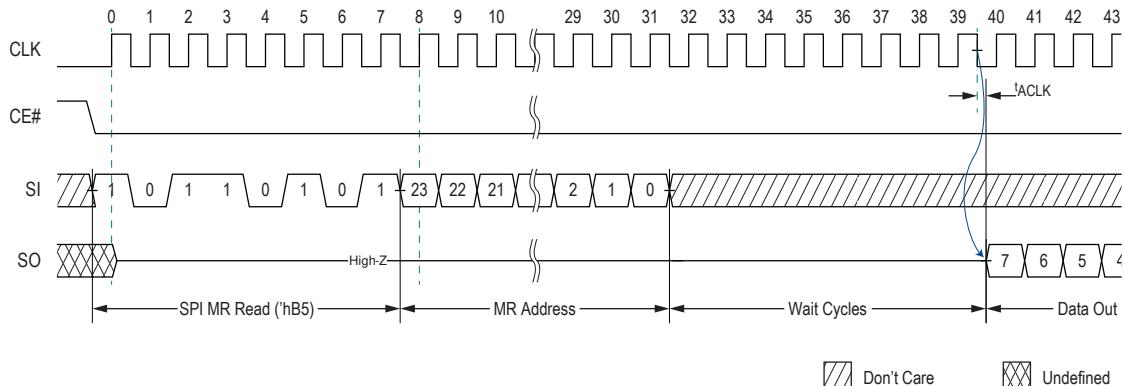
Figure 4: SPI MR Read 'hB5

12.2 SPI MR Write Operation
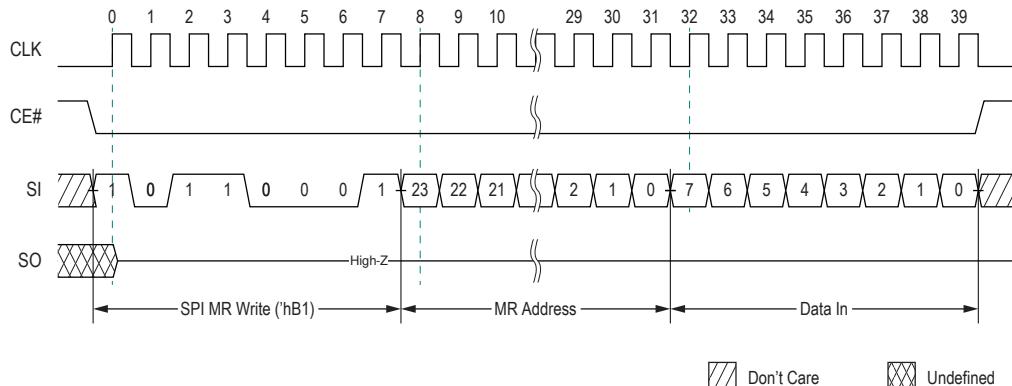
Figure 5: SPI MR Write 'hB1

12.3 QPI MR Read Operation

For all reads, MR data will be available ^{t}ACLK after the falling edge of CLK.
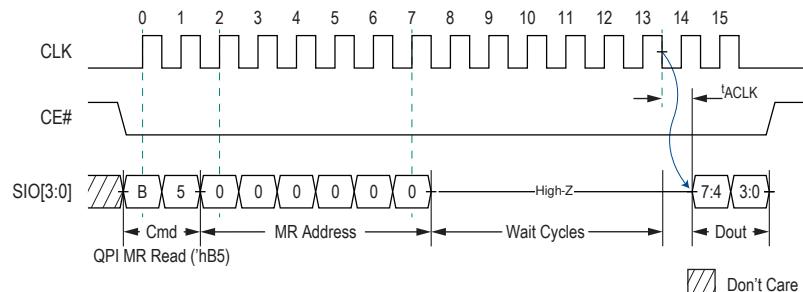
Figure 6: QPI MR Read 'hB5

12.4 QPI MR Write Operation
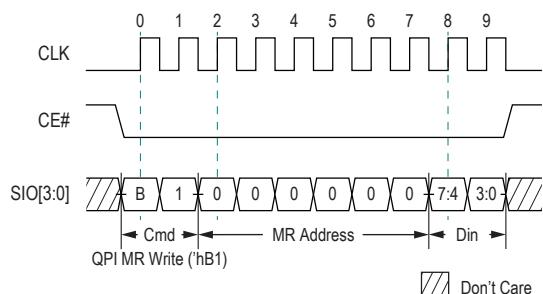
Figure 7: QPI MR Write 'hB1

13 Read ID

Read ID command provides information of vendor ID, known-good-die, device density, and manufacturing ID. It can be executed under the following 2 conditions: (Please see the following Figure 8)

1. Run it as the first operation after power up and before any other commands being executed.
2. Issue a memory read command with address = 'h00000 first, then Read ID command.
3. Issue a pre-condition of dummy read id, then Read ID command.
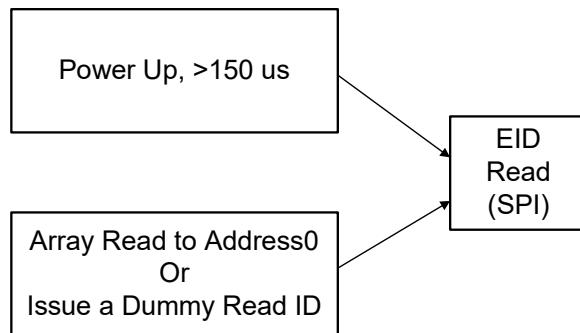
Figure 8: Pre-condition of EID Read

13.1 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.
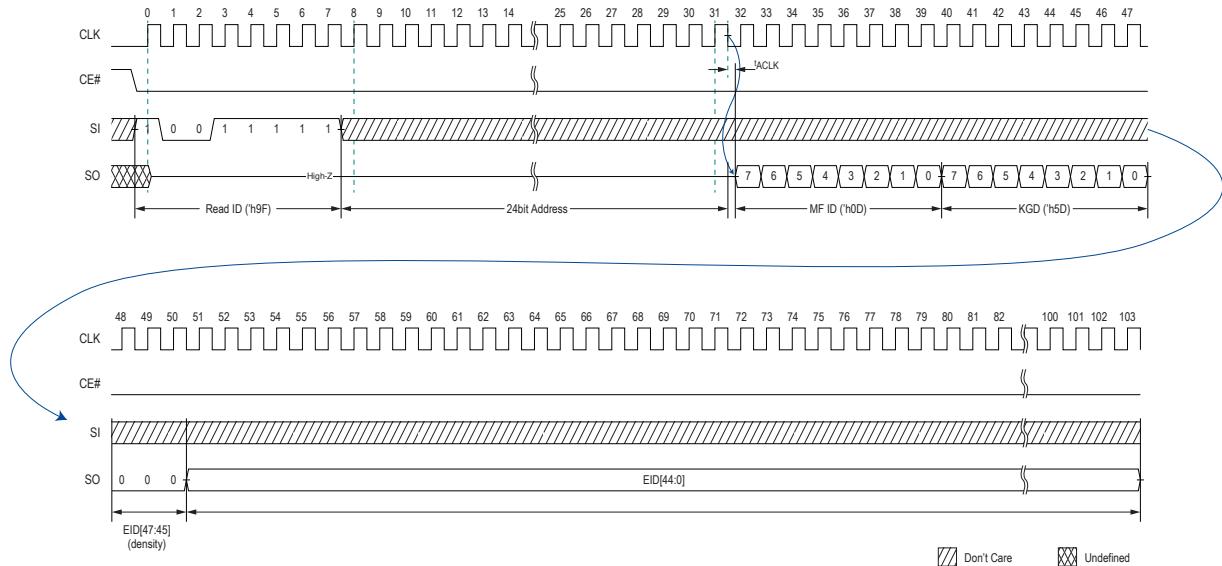
Figure 9: SPI Read ID 'h9F (available only in SPI mode)

13.2 QPI Read ID Operation

In QPI mode Read ID command is basically an QPI MR Read, but with particular attention to the Dout[7]. MRR data out bit[7] outputs serial ID data which is repeated every two clocks.
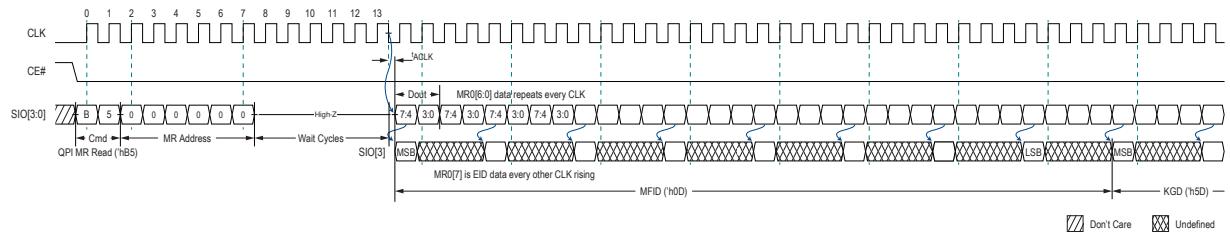

Figure 10: QPI Read ID (MR Read 'hB5) (max freq 84MHz)

Table 6: Known Good Die (KGD)

KGD[7:0]	Known Good Die
'b0101_0101	FAIL
'b0101_1101	PASS

*Note: Default is FAIL die, and only mark PASS after all tests passed.

14 Toggle Burst Length Operation

The Toggle Burst Length Operation switches the device's wrapped burst boundary between the Mode Register setting (default of 512 bytes CA[8:0]) and 32 (CA[4:0]) bytes or whatever is set in MR0[6:5] and a fixed value of 32 bytes.
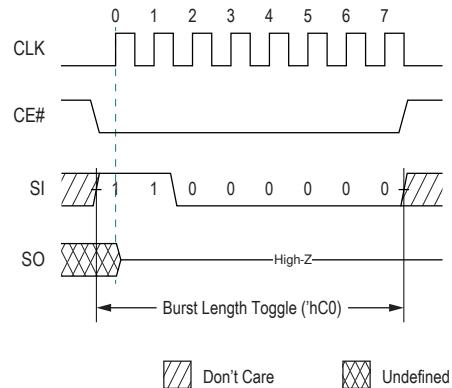
Figure 11: SPI Burst Length Toggle 'hC0
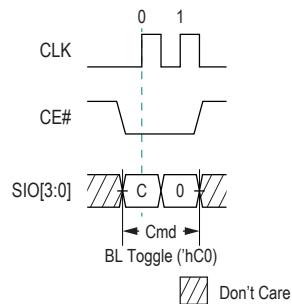
Figure 12: QPI Burst Length Toggle 'hC0

15 SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

15.1 SPI Read Operations

For all reads, data will be available ^{t}ACLK after the falling edge of CLK.

SPI Reads can be done in four ways:

1. 'h03: Serial CMD, Serial Addr/IO, slow frequency

2. 'h0B: Serial CMD, Serial Addr/IO, fast frequency

3.   'hEB: Serial CMD, Quad Addr/IO, fast frequency

4. 'h8B: Serial CMD, Serial Addr/IO, fast frequency
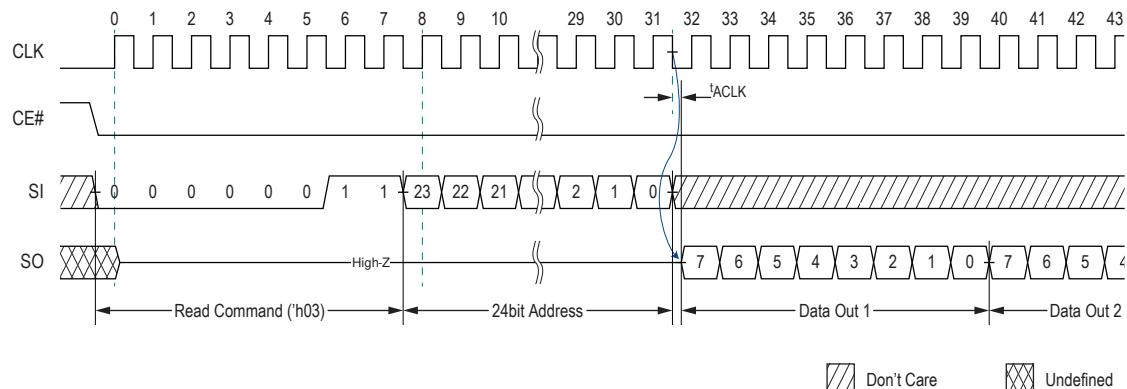

Figure 13: SPI Read 'h03 (max freq 33MHz)
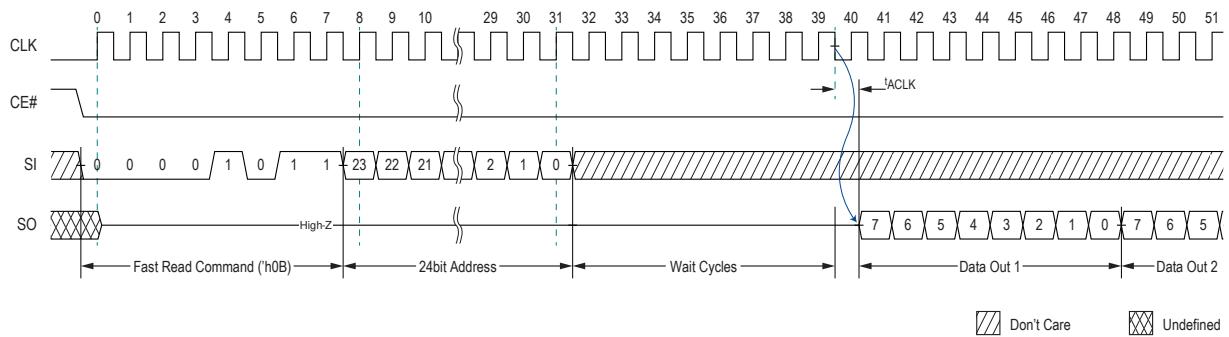
**Figure 14: SPI Fast Read 'h0B (max freq 144 MHz)**
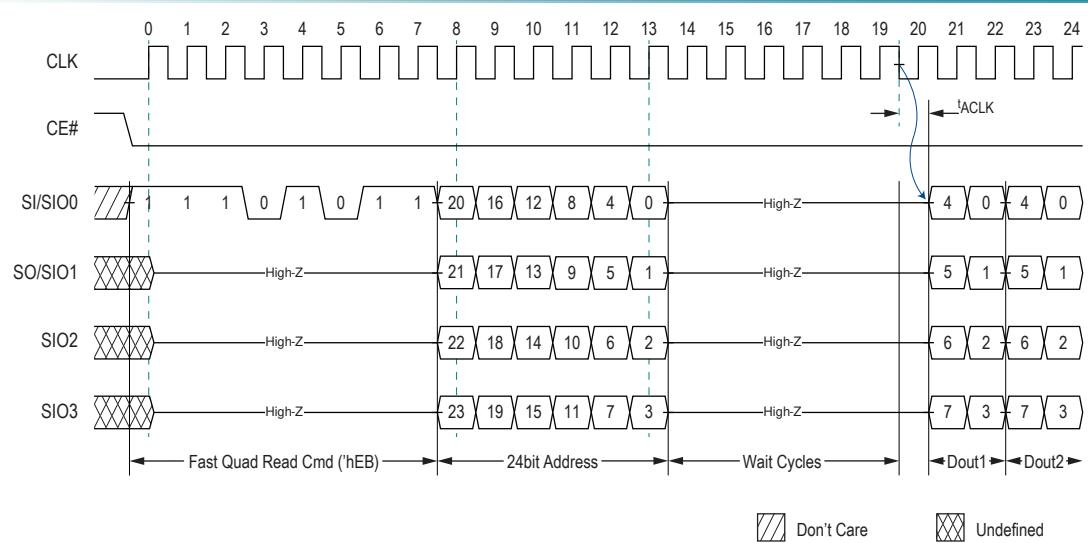
Figure 15: SPI Fast Quad Read 'hEB (max freq 144 MHz)

15.2 SPI Write Operations
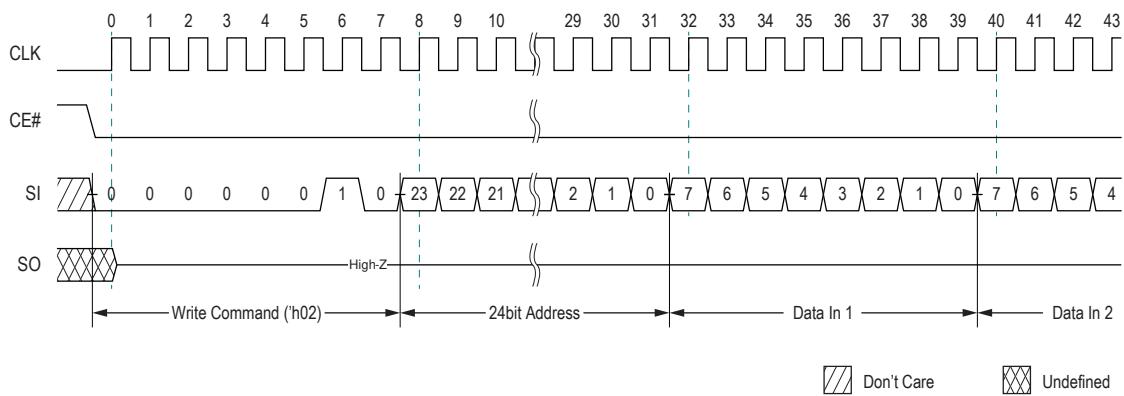

Figure 16: SPI Write 'h02
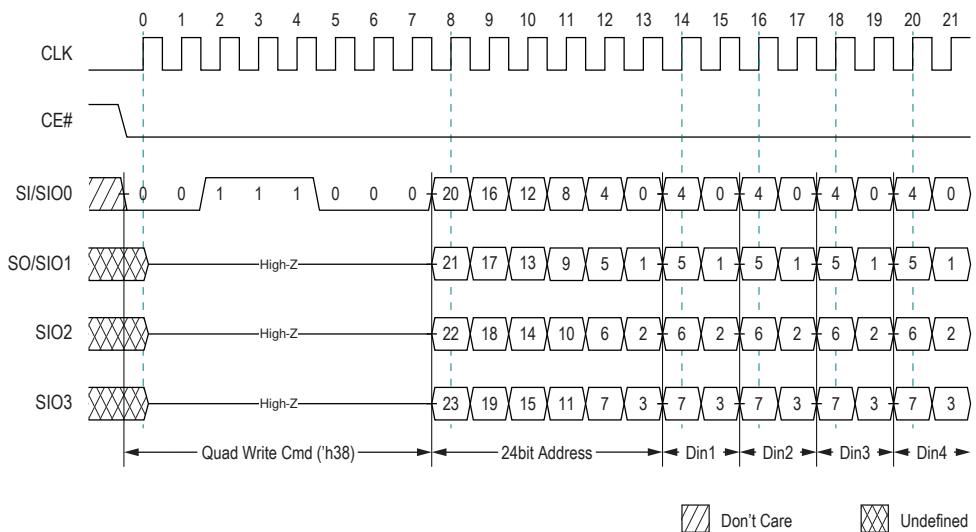
Figure 17: SPI Quad Write 'h38

15.3 SPI Quad Mode Enable Operation

This command switches the device into quad IO mode.
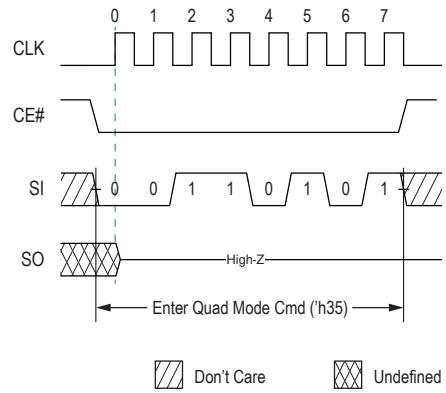
Figure 18: Quad Mode Enable 'h35 (available only in SPI mode)

16 QPI Mode Operations

16.1 QPI Read Operations

For all reads, data will be available ^tACLK after the falling edge of CLK.

QPI Reads can be done in one of three ways:

1. 'h0B: Quad CMD, Addr & IO , slow frequency.

2. 'hEB: Quad CMD, Addr & IO, fast frequency.

3. 'h8B: Quad CMD, Addr & IO,fast frequency.
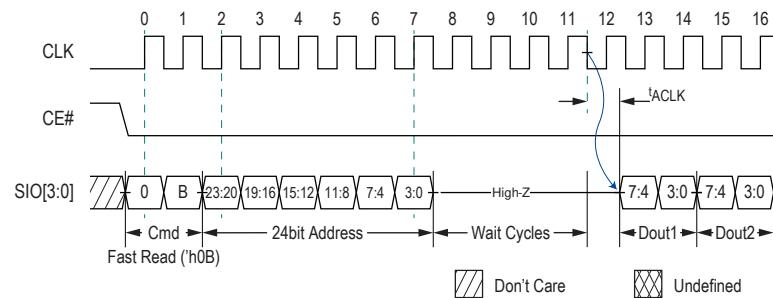
Figure 19: QPI Fast Read 'h0B (max freq 66 MHz)
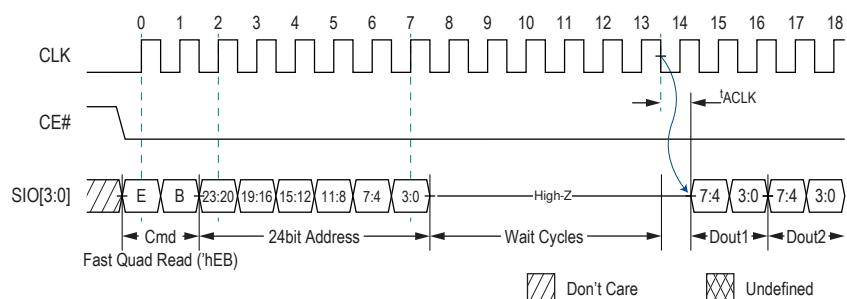
Figure 20: QPI Fast Quad Read 'hEB (max freq 144 MHz)

16.2 QPI Write Operation(s)

QPI write command can be done in one of two ways:

1. 'h02 or 'h38: Quad CMD, Addr & IO.

2. 'h82:   Quad CMD, Addr & IO.
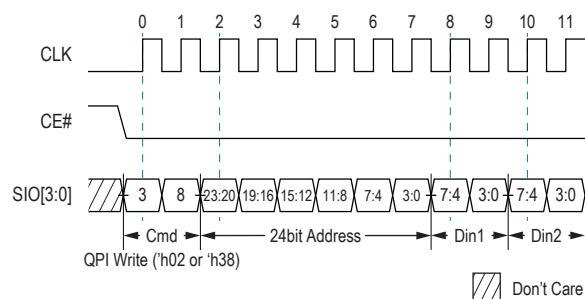
Figure 21: QPI Write

16.3 QPI Quad Mode Exit operation

This command will switch the device back into serial IO mode.
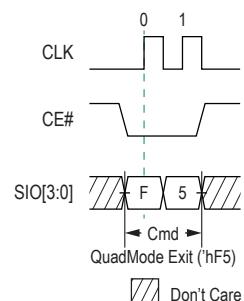
Figure 22: Quad Mode Exit 'hF5 (only available in QPI mode)

17   Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).
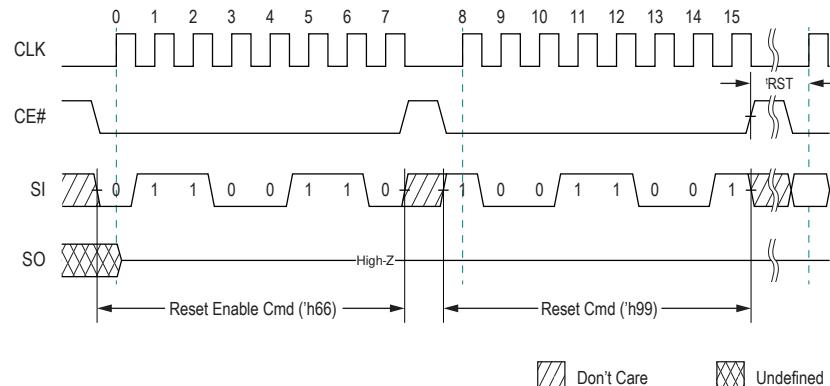

Figure 23: SPI Reset
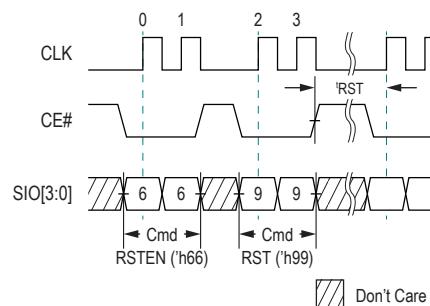
Figure 24: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

18 Input/Output Timing
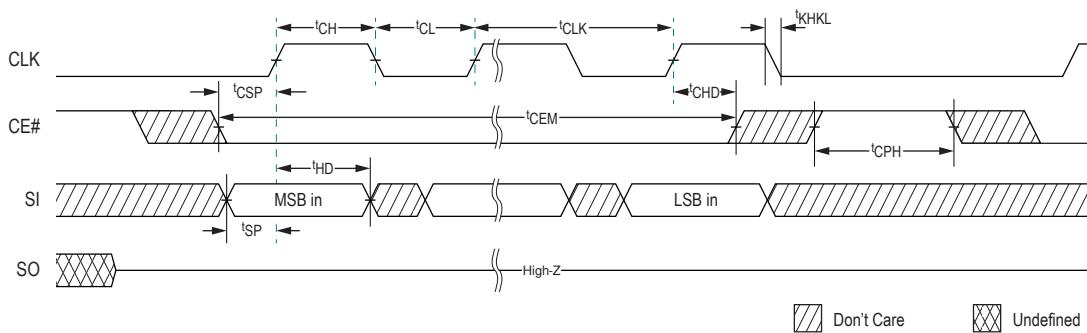
Figure 25: Input Timing
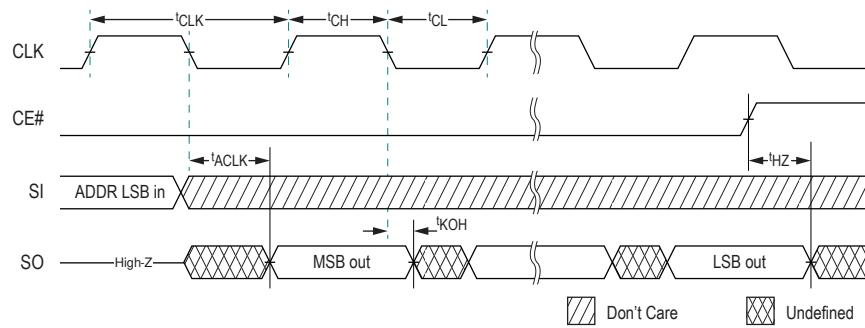
Figure 26: Output Timing

19 Electrical Specifications:

19.1 Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

| Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except V_{DD} relative to V_{SS}	VT	-0.4 to V_{DD}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes   1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

19.2 Pin Capacitance

Table 8: Bare Die Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note   1: spec'd at 25°C.

Table 9: Package Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note   1: spec'd at 25°C.

Table 10: Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C_L		15	pF	

Note   1: System C_L for the use of package

19.3 Decoupling Capacitor Requirement

It is required to have a decoupling capacitor on VDD pin for IO switchings and psram internal transient events. A low ESR 1µF ceramic cap is recommended. To minimize parasitic inductance, place the cap as close to VDD pin as possible. An optional 0.1µF can further improve high frequency transient response.
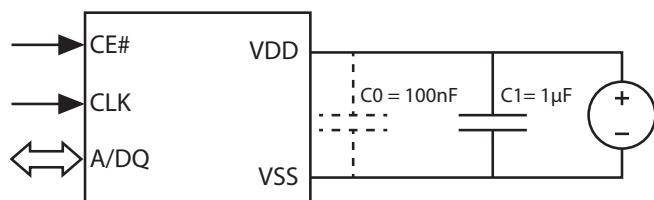
Figure 27: Decoupling Capacitor

Note that the length of grounding connection between PSRAM and PCB must be as short as possible. Having **ground plane on PCB** and **multipoint ground** would be preferred (to avoid single-point grounding topology). The width of VDD and VSS traces would be suggested more than 20mil.

19.4 Operating Conditions

Table 11: Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	1
Operating Temperature (standard)	-40(-25*)	85	°C	*varies by package type

Note   1: spec'd temp range of -40 to 105°C is only characterized; test condition will be -32 to 105°C.

19.5 DC Characteristics

Table 12: DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DD}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
I_{CC}	Read/Write (144MHz)		7	mA	1,2
	Read/Write (66MHz)		6	mA	1,2
	Read/Write (13MHz)		5	mA	1,2
ISB_{EXT}	Standby current (extended temp)		150	µA	3
ISB_{STD}	Standby current (standard temp)		100	µA	3
$ISB_{STDRoom}$	Standby current (standard room temp)		25	µA	3,4

Note   1: Output load current not included.

2: Typical Icc 5mA.

3: Standby current is measured when CLK is in DC low state.

4: Typical ISBSTD 20µA at 25°C

19.6 AC Characteristics

Table 13: READ/WRITE Timing

Symbol	Parameter	Min	Max	Unit	Notes
^{t}CLK	CLK period - SPI Read ('h03)	30.3		ns	33MHz
	CLK period - QPI Read ('h0B)	15.1			66MHz
	CLK period - all other operations	7			144MHz[*1,2,3]
^{t}CH/^{t}CL	Clock high/low width	0.45	0.55	^{t}CLK(min)	
^{t}KHKL	CLK rise or fall time		1.1	ns	4
^{t}CPH	CE# HIGH between subsequent burst operations	18		ns	
^{t}CEM	CE# low pulse width		4	µs	Extended grade
			8		Standard grade
^{t}CSP	CE# setup time to CLK rising edge PKG	2.5		ns	2
^{t}CHD	CE# hold time from CLK rising edge PKG	3		ns	2
^{t}SP	Setup time to active CLK edge	2		ns	
^{t}HD	Hold time from active CLK edge	2		ns	
^{t}HZ	Chip disable to DQ output high-Z		6	ns	
^{t}ACLK	CLK to output delay	2	5.5	ns	3
^{t}KOH	Data hold time from clock falling edge	1.5		ns	
^{t}RST	Time between end of RST CMD to next valid CMD	50		ns	

Note   1: Frequency limit of wrapped type bursts are therefore 144MHz max

2: System max C_L 15pF for the use of package.

3: For operating frequencies >84MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).

4: Measured from 20% to 80% of VDD

20 Change Log

Version	Date	Description
0.1	December 23, 2016	Initial Version
0.2	May 11, 2017	Added linear bursting, page toggle cmds; updated ISB current and timing parameters for 144MHz; removed QPI Read 'h0B support; clarified termination section; added pin cap tables
1.0	May 31, 2017	Modified linear burst to wrapped bursting
1.1	July 10, 2017	added Typical current #, tCPH update
1.2	Aug 24, 2017	Corrected package code; Added system max C_L for the use of package & related tCK and tCHD; relaxed tCSP/tHD, removed drive strength setting '11, changed tACLK, tKHKL; added note to ICC & ordering information of package
1.5	Oct 30, 2017	Enabled QPI Read 'h0B support; changed Min/Max absolute voltage, Vil_min and Vih_max,; defined tCEM for different temperature grade; corrected speed typo. Added USON package ZR, ISBstd@25C
1.6	Nov 10, 2017	Modified spec of ISB, ICC
1.7	Feb 26, 2018	Typo corrected in Fig.12, 17
1.8	Mar 28, 2018	RBX not supported, temperature grade -40C
1.9	June 12, 2018	Corrected linear burst to wrap bursting 512
2.0	Nov. 20, 2018	Revised speed for Read ID and ordering information for package code ZR temperature(-25C); deleted Package Outline Drawing - WSON-8L 6x5mm, (package code ZP); revised USON code "ZR"Delete SIP related information
2.1	Dec. 6, 2018	Added SPI MRW/MRR waves, QPI EID Read, corrected some wording, tRST parameter, Block Diagram; updated POD of USON, POD of USON with PIN#.
2.2	Jan. 10, 2019	Update L1/L2 value of USON
2.3	Jan. 11, 2019	Update L1/L2 value of USON again
2.4	Aug. 19, 2019	Updated Section 13 Read ID
2.5a	Oct 02, 2019	Updated header, footer, page 1 and the format of Change Log; added Section 19.3; Updated Table 1, section 11 and section 19.6
2.6	Oct 24, 2019	Updated typo in 16.1 and the table in section 11; updated Table 11: Operating CharacteristicsTable 11 and notes in 19.3
2.7	Nov 21, 2019	Updated Table 2