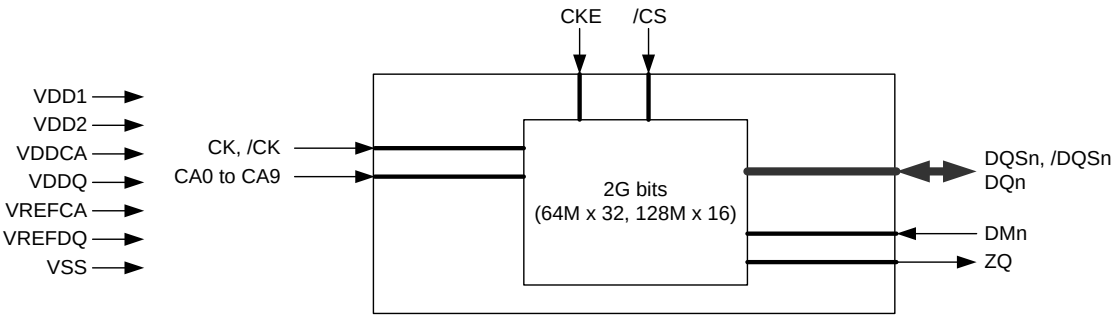
2Gb LPDDR2 Specification

Specifications

- **Density**: 2G bits
- **Organization**
  - 8 banks x 16M words x 16 bits
  - 8 banks x 8M words x 32 bits
- **Power Supply**
  - VDD1=1.7 to 1.95V
  - VDD2,VDDCA,VDDQ=1.14 to 1.3V
- **Clock frequency**: 466/400/333/266/200/166 MHz
- **2KB Page Size**
  - Row address: AX0 to AX13
  - Column address: AY0 to AY9 (X 16 bits)
  - Column address: AY0 to AY8 (X 32 bits)
- **Eight Internal Banks for Concurrent Operation**
- **Interface**: HSUL_12
- **Burst Lengths** (BL): 4, 8, 16
- **Burst Type (BT)**
  - Sequential (4, 8, 16)
  - Interleave (4, 8)
- **Read Latency (RL)**: 3, 4, 5, 6**,** 7, 8
- **Write Latency (WL)**: 1, 2, 3, 4
- **Precharge**: auto precharge option for each burst access
- **Programmable Driver Strength**
- **Refresh**: auto-refresh, self-refresh
- **Refresh Cycles**: 8132 cycles/32ms
- **Average Refresh Period**: 3.9µs
- **Operating Temperature Range**
  - TC = -25°C to +85°C

Features

- DLL is not implemented
- Low power consumption
- JEDEC LPDDR2-S4B compliance
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture
- Differential clock inputs (CK and /CK)
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data



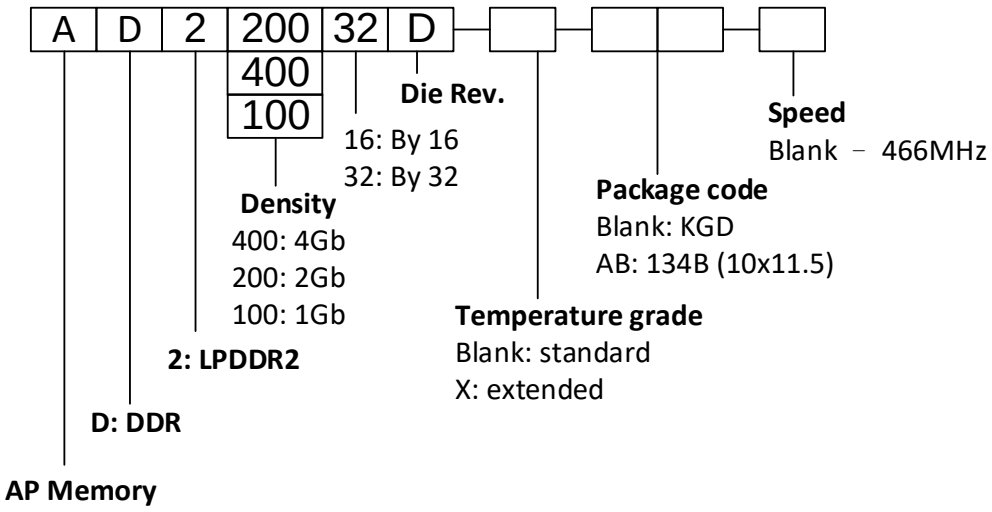
Differences from JEDEC:

1) Mode Register 9, bit [5] is a readable Failed Die Bit.

Table of Contents

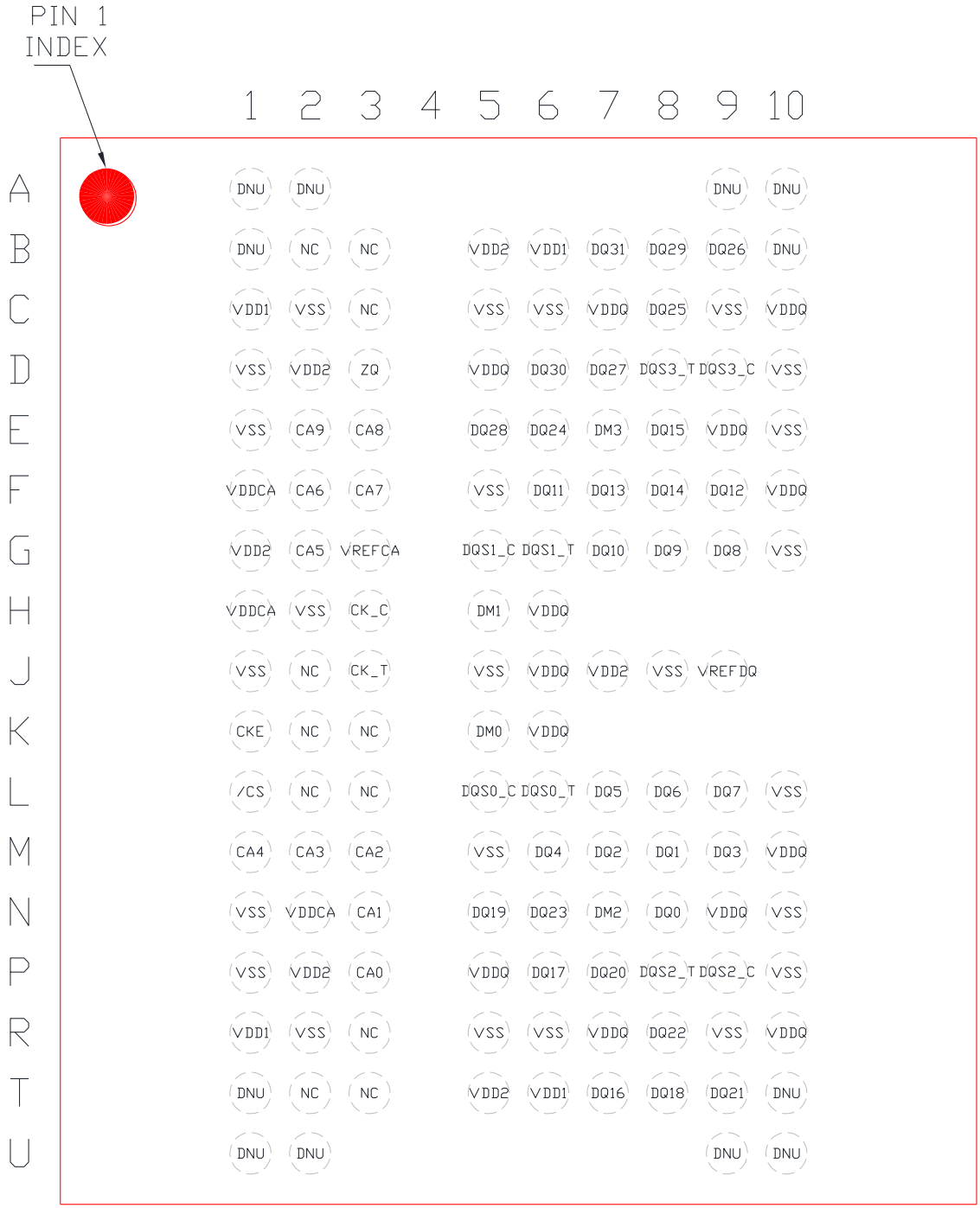
1 Ordering Information

Part Number	*Configuration*	*Temperature Range*	*Max Frequency*	*Note*
AD220032D-AB	X32	-25°C to +85°C	466 MHz	134B (10x11.5)
AD220016D-AB	X16	-25°C to +85°C	466 MHz	134B (10x11.5)



2 Package Ball Assignment:

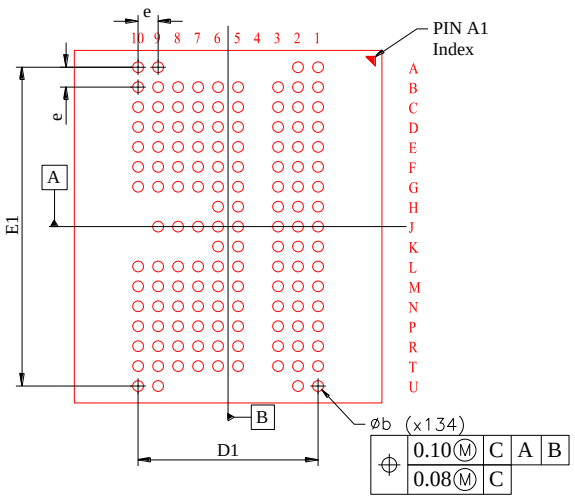
2.1 x32/16: "134-Ball FBGA –10x11.5x1.0 mm, ball pitch 0.65 mm, ball size 0.4 mm. (package code AB)"



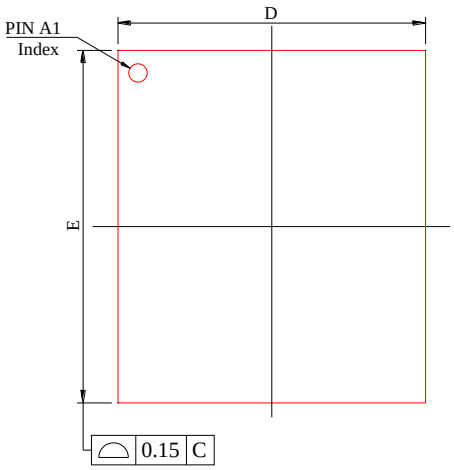
Top View Through Package

3 Package Outline Drawing:

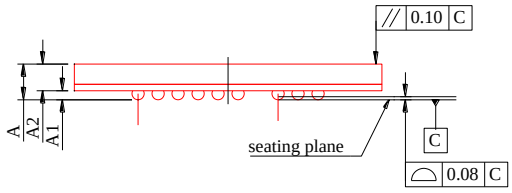
3.1 x32/16 : "134-Ball FBGA –10x11.5x1.0 mm, ball pitch 0.65 mm, ball size 0.4 mm. (package code AB)"



Bottom View



Top View



Side View

Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.27	0.32	0.37
A2	0.545	0.58	0.63
D	9.90	10.00	10.10
D1		5.85 BSC	
E	11.40	11.50	11.60
E1		10.40 BSC	
b	0.35	0.40	0.45
e		0.65 BSC	

4 Electrical Specifications:

All voltages are referenced to each GND level (VSS, VSSCA, and VSSQ).
Execute power-up and Initialization sequence before proper device operation can be achieved.

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on any pin relative to VSSCA, VSSQ	VT	-0.4 to +1.6	V	
Power supply voltage (core power1) relative to VSS	VDD1	-0.4 to +2.3	V	
Power supply voltage (core power2) relative to VSS	VDD2	-0.4 to +1.6	V	
Power supply voltage for command, address relative to VSSCA	VDDCA	-0.4 to +1.6	V	
Power supply voltage for output relative to VSSQ	VDDQ	-0.4 to +1.6	V	
Storage temperature	Tstg	-55 to +125	°C	1
Power dissipation	PD	1.0	W	
Short circuit output current	IOUT	50	mA	

Notes:
Storage temperature the case surface temperature on the center/top side of the DRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

4.2 Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	-25 to +85	˚C	1

Notes 1:
Operating temperature is the case surface temperature on the center/top side of the DRAM.
Refer to MR4 programing table for Temperature Sensor de-rating & refresh rate numbers.

4.3 Recommended DC Operating Conditions

(TC = -25°C to +85°C)

Parameter		Symbol	min.	typical	max	Unit	Notes
Supply voltage	core power1	VDD1	1.7	1.8	1.95	V	1
		VSS	0	0	0	V	
	core power2	VDD2	1.14	1.2	1.3	V	1
		VSS	0	0	0	V	
	for command, address	VDDCA	1.14	1.2	1.3	V	1
		VSSCA	0	0	0	V	
	for output	VDDQ	1.14	1.2	1.3	V	1
		VSSQ	0	0	0	V	

Notes:
VDDQ tracks with VDD2, VDDCA tracks with VDD2. AC parameters are measured with VDD2, VDDCA and VDDQ tied together.

4.4 AC and DC Input Measurement Levels

[Refer to section 8 in JEDEC Standard No. 209-2E]

4.5 DC Characteristics 1

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Test Condition	Symbol	Power Supply	Max						Unit
				DDR 933	DDR 800	DDR 667	DDR 533	DDR 400	DDR 333	
Operating one bank active-precharge current	tCK = tCK(min); tRC = tRC(min); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$	VDD1	10						mA
		$IDD0_2$	VDD2	50						mA
		$IDD0_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
Idle power-down standby current	tCK = tCK(min); CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$	VDD1	0.4						mA
		$IDD2P_2$	VDD2	1.8						mA
		$IDD2P_{IN}$	VDDCA	0.1						mA
			VDDQ	0.2						mA
Idle power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bust inputs are STABLE;	$IDD2PS_1$	VDD1	0.4						mA
		$IDD2PS_2$	VDD2	1.8						mA
		$IDD2PS_{IN}$	VDDCA	0.1						mA
			VDDQ	0.2						mA
Idle non power-down standby current	tCK = tCK(min); CKE is HIGH; CS_n is HIGH, all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$	VDD1	0.6						mA
		$IDD2N_2$	VDD2	15						mA
		$IDD2N_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
Idle non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2NS_1$	VDD1	0.6						mA
		$IDD2NS_2$	VDD2	8						mA
		$IDD2NS_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
Active power-down standby current	tCK = tCK(min); CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	VDD1	1						mA
		$IDD3P_2$	VDD2	10						mA
		$IDD3P_{IN}$	VDDCA	0.1						mA
			VDDQ	0.2						mA
Active power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3PS_1$	VDD1	1						mA
		$IDD3PS_2$	VDD2	10						mA
		$IDD3PS_{IN}$	VDDCA	0.1						mA
			VDDQ	0.2						mA
Active non power-down standby current	tCK = tCK(min); CKE is HIGH; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	VDD1	1.5						mA
		$IDD3N_2$	VDD2	20						mA
		$IDD3N_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
Active non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3NS_1$	VDD1	1.5						mA
		$IDD3NS_2$	VDD2	15						mA
		$IDD3NS_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA

Parameter	Test Condition	Symbol	Power Supply	Max						Unit
				DDR 933	DDR 800	DDR 667	DDR 533	DDR 400	DDR 333	
Operating burst read current	tCK = tCK(min); CS_n is HIGH between valid commands; one bank active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING;	$IDD4R_1$	VDD1	2						mA
		$IDD4R_2$	VDD2	200	195	190	165	130	110	mA
		$IDD4R_{IN}$	VDDCA	6.5						mA
Operating burst write current	tCK = tCK (min); CS_n is HIGH between valid commands; one bank active; BL = 4; WL = WL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	2						mA
		$IDD4W_2$	VDD2	265	210	190	160	110	100	mA
		$IDD4W_{IN}$	VDDCA	6.5						mA
			VDDQ	30						mA
All Bank Auto Refresh Burst Current	tCK = tCK (min); CS_n is HIGH between valid commands; tRC = tRFCab(min); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5_1$	VDD1	35						mA
		$IDD5_2$	VDD2	143						mA
		$IDD5_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
All Bank Auto Refresh Average Current	tCK = tCK(min); CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputsa are STABLE	$IDD5ab_1$	VDD1	2						mA
		$IDD5ab_2$	VDD2	18						mA
		$IDD5ab_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
Per Bank Auto Refresh Average Current	tCK = tCK(min); CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5pb_1$	VDD1	2						mA
		$IDD5pb_2$	VDD2	18						mA
		$IDD5pb_{IN}$	VDDCA	6.5						mA
			VDDQ	1						mA
Self Refresh Current (Standard Temerature Range: -30˚C to 85˚C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1 x Self-refresh rate	$IDD6_1$	VDD1	850						µA
		$IDD6_2$	VDD2	3.5						mA
		$IDD6_{IN}$	VDDCA	100						µA
			VDDQ	200						µA
Deep Power Down Current (Standard Temerature Range: -30˚C to 85˚C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD8_1$	VDD1	300						µA
		$IDD8_2$	VDD2	600						µA
		$IDD8_{IN}$	VDDCA	70						µA
			VDDQ	200						µA
Self Refresh Current (Extended Temerature Range: 85˚C to 105˚C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD6ET_1$	VDD1	3						mA
		$IDD6ET_2$	VDD2	10						mA
		$IDD6ET_{IN}$	VDDCA	100						µA
			VDDQ	300						µA
Deep Power Down Current (Extended Temerature Range: 85˚C to 105˚C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD8ET_1$	VDD1	300						µA
		$IDD8ET_2$	VDD2	1						mA
		$IDD8ET_{IN}$	VDDCA	70						µA
			VDDQ	200						µA

4.6 Advanced Data Retention Current (Self-refresh current)

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter		Symbol	supply	Typical	Unit	Test Condition
+25°C CKE ≤ 0.2V	Full Array	$IDD6_1$	VDD1	192	µA	All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		$IDD6_2$	VDD2	600	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	10		
	1/2 Array	$IDD6_1$	VDD1	144	µA	
		$IDD6_2$	VDD2	400	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	10		
	1/4 Array	$IDD6_1$	VDD1	120	µA	
		$IDD6_2$	VDD2	300	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	10		
	1/8 Array	$IDD6_1$	VDD1	108	µA	
		$IDD6_2$	VDD2	248	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	10		
+45°C CKE ≤ 0.2V	Full Array	$IDD6_1$	VDD1	240	µA	
		$IDD6_2$	VDD2	760	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	15		
	1/2 Array	$IDD6_1$	VDD1	176	µA	
		$IDD6_2$	VDD2	520	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	15		
	1/4 Array	$IDD6_1$	VDD1	144	µA	
		$IDD6_2$	VDD2	384	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	15		
	1/8 Array	$IDD6_1$	VDD1	128	µA	
		$IDD6_2$	VDD2	320	µA	
		$IDD6_{IN}$	VDDCA	1	µA	
			VDDQ	15		

Parameter		Symbol	supply	max	Unit	Test Condition
+45°C ≤ TC ≤ +85°C CKE ≤ 0.2V	Full Array	$IDD6_1$	VDD1	0.85	mA	All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		$IDD6_2$	VDD2	3.5	mA	
		$IDD6_{IN}$	VDDCA	100	µA	
			VDDQ	200		
	1/2 Array	$IDD6_1$	VDD1	0.75	mA	
		$IDD6_2$	VDD2	3	mA	
		$IDD6_{IN}$	VDDCA	100	µA	
			VDDQ	200		
	1/4 Array	$IDD6_1$	VDD1	0.65	mA	
		$IDD6_2$	VDD2	2.7	mA	
		$IDD6_{IN}$	VDDCA	100	µA	
			VDDQ	200		
	1/8 Array	$IDD6_1$	VDD1	0.6	mA	
		$IDD6_2$	VDD2	2.5	mA	
		$IDD6_{IN}$	VDDCA	100	µA	
			VDDQ	200		

Notes:

1) This device supports both bank-masking and segment-masking. IDD6 PASR currents are measured using bank-masking only.
2) IDD6 85°C is the maximum and IDD6 25°C/45°C are typical of the distribution of the arithmetic

4.7 DC Characteristics 2

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min.	max	Unit	Test Condition	Notes
Input leakage current	ILI	-2.0	2.0	µA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	-1.5	1.5	µA	0 ≤ VOUT ≤ VDDQ DQ = disable	
Output high voltage	VOH	0.9×VDDQ	--	V	IOH = -0.1mA	
Output low voltage	VOL	--	0.1×VDDQ	V	IOL = 0.1mA	

4.8 DC Characteristics 3

(TC = -25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min.	max	Unit	Notes
AC differential input voltage	VID (AC)	-0.2	VDDQ + 0.2	V	
AC differential cross point voltage	VIX (AC)	0.5 x VDDQ - 0.15	0.5 x VDDQ + 0.15	V	
AC differential cross point voltage	VOX (AC)	0.5 x VDDQ - 0.2	0.5 x VDDQ + 0.2	V	

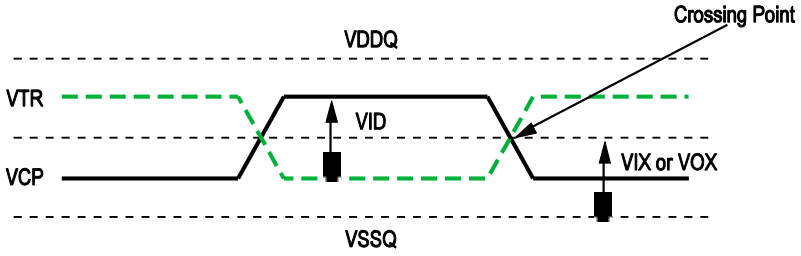


Figure 1. Differential Signal Levels

4.9 Pin Capacitance

(TA = +25°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol		LPDDR2 933-466	LPDDR2 400-200	Unit	Notes
CLK input pin capacitance CK, /CK	CCK	min.	1.0		pF	1,2
		max	2.0			
CLK input pin capacitance Δ CK, /CK	CDCK	min.	0		pF	1,2,3
		max	0.20	0.25		
Input pin capacitance CA, /CS, CKE	CI	min.	1.0		pF	1,2,4
		max	2.0			
Input pin capacitance Δ CA, /CS, CKE	CDI	min.	-0.4	-0.5	pF	1,2,5
		max	0.4	0.5		
Input/output pin capacitance DQS, /DQS, DQ, DM	CIO	min.	1.25		pF	1,2,6,7
		max	2.5			
Input/output pin capacitance Δ DQS, /DQS	CDDQS	min.	0		pF	1,2,7,8
		max	0.25	0.30		
Input/output pin capacitance Δ DQ, DM	CDIO	min.	-0.5	-0.6	pF	1,2,7,9
		max	0.5	0.6		
Calibration pin capacitance	CZQ	min.	0		pF	1,2
		max	2.5			

Notes:

1) This parameter applies to die device only (does not include package capacitance)
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3) Absolute value of CCK_t-CCK_c.
4) CI applies to /CS, CKE, CA0-CA9.
5) CDI=CI-0.5x(CCK_t+CCK_c)
6) DM loading matches DQ and DQS
7) MR3 I/O configuration DS OP3-OP0=4'b0001 (34.3Ω typical)
8) Absolute value of CDQS_t and CDQS_c.
9) CDIO=CIO-0.5x(CDQS_t+CDQS_c) in byte-lane.

4.10 Refresh Requirement Parameters (2Gb)

Parameter	Symbol	Value	Unit
Number of Banks		8	
Refresh Window Tcase ≤ 85°C	t_{REFW}	32	ms
Refresh Window Tcase 85°C < Tcase ≤ 105°C	t_{REFW}	8	ms
Required number of REFRESH commands (min)	R	8,192	
average time between REFRESH commands	t_{REFI}	3.9	µs
Refresh Cycle time	t_{RFCab}	130	ns
Per Bank Refresh Time	t_{RFCpb}	60	ns
Burst Refresh Window = 4 x 8 x t_{RFC}	t_{REFBW}	4.16	µs

4.11 AC Characteristics

(TC = –25°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min/max	min t_{CK}	LPDDR2						Unit
				933	800	667	533	400	333	Mbps
Max. Frequency		~		466	400	333	266	200	166	MHz
Clock Timing										
Average Clock Period	$t_{CK}(avg)$	min		2.15	2.5	3	3.75	5	6	ns
		max		100						
Average high pulse width	$t_{CH}(avg)$	min		0.45						$t_{CK}(avg)$
		max		0.55						
Average low pulse width	$t_{CL}(avg)$	min		0.45						$t_{CK}(avg)$
		max		0.55						
Absolute Clock Period	$t_{CK}(abs)$	min		$t_{CK}(avg)(min) + t_{JIT}(per)(min)$						ps
Absolute clock HIGH pulse width (with allowed jitter)	$t_{CH}(abs)$	min		0.43						$t_{CK}(avg)$
		max		0.57						
Absolute clock LOW pulse width (with allowed jitter)	$t_{CH}(abs)$	min		0.43						$t_{CK}(avg)$
		max		0.57						
Clock Period Jitter (with allowed jitter)	$t_{JIT}(per)$	min		-95	-100	-110	-120	-140	-150	ps
		max		95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	$t_{JIT}(cc)$	max		190	200	220	240	280	300	ps
Duty cycle Jitter (with allowed jitter)	$t_{JIT}(duty)$ allowed	min		$\min((t_{CH}(abs),min - t_{CH}(avg),min) (t_{CL}(abs), min - t_{CL}(avg), min)) \times t_{CK}(avg)$						ps
		max		$\max((t_{CH}(abs),max - t_{CH}(avg),max) (t_{CL}(abs), max - t_{CL}(avg), max)) \times t_{CK}(avg)$						
Cumulative error across 2 cycles	$t_{ERR}(2per)$ allowed	min		-140	-147	-162	-177	-206	-221	ps
		max		140	147	162	177	206	221	
Cumulative error across 3 cycles	$t_{ERR}(3per)$ allowed	min		-166	-175	-192	-210	-245	-262	ps
		max		166	175	192	210	245	262	
Cumulative error across 4 cycles	$t_{ERR}(4per)$ allowed	min		-185	-194	-214	-233	-272	-291	ps
		max		185	194	214	233	272	291	
Cumulative error across 5 cycles	$t_{ERR}(5per)$ allowed	min		-199	-209	-230	-251	-293	-314	ps
		max		199	209	230	251	293	314	
Cumulative error across 6 cycles	$t_{ERR}(6per)$ allowed	min		-210	-222	-244	-266	-311	-333	ps
		max		210	222	244	266	311	333	
Cumulative error across 7 cycles	$t_{ERR}(7per)$ allowed	min		-221	-232	-256	-279	-325	-348	ps
		max		221	232	256	279	325	348	

Parameter	Symbol	min/max	min t_{CK}	LPDDR2						Unit
				933	800	667	533	400	333	Mbps
Cumulative error across 8 cycles	t_{ERR}(8per) allowed	min		-229	-241	-256	-290	-338	-362	ps
		max		229	241	256	290	338	362	
Cumulative error across 9 cycles	t_{ERR}(9per) allowed	min		-237	-249	-274	-299	-349	-374	ps
		max		237	249	274	299	349	374	
Cumulative error across 10 cycles	t_{ERR}(10per) allowed	min		-244	-257	-282	-308	-359	-385	ps
		max		244	257	282	308	359	385	
Cumulative error across 11 cycles	t_{ERR}(11per) allowed	min		-250	-263	-289	-316	-368	-395	ps
		max		250	263	289	316	368	395	
Cumulative error across 12 cycles	t_{ERR}(12per) allowed	min		-256	-269	-296	-323	-377	-403	ps
		max		256	269	296	323	377	403	
Cumulative error across n = 13, 14 … 49, 50 cycles	t_{ERR}(nper) allowed	min		t_{ERR}(nper), allowed, min = (1 + 0.68ln(n)) x t_{JIT}(per), allowed, min						ps
		max		t_{ERR}(nper), allowed, max = (1 + 0.68ln(n)) x t_{JIT}(per), allowed, max						
ZQ Calibration Parameters										
Initialization Calibration Time	t_{ZQINIT}	min		1						µs
Long Calibration Time	t_{ZQCL}	min	6	360						ns
Short Calibration Time	t_{ZQCS}	min	6	90						ns
Calibration Reset Time	$t_{ZQRESET}$	min	3	50						ns
Read Parameters										
DQS output access time from CK_t/CK_c	t_{DQSCK}	min		2500						ps
		max		5500						
DQSCK Delta Short	$t_{DQSCKDS}$	max		380	450	540	670	900	1080	ps
DQSCK Delta Medium	$t_{DQSCKDM}$	max		780	900	1050	1350	1800	1900	ps
DQSCK Delta Long	$t_{DQSCKDL}$	max		1050	1200	1400	1800	2400	-	ps
DQS-DQ skew	t_{DQSQ}	max		220	240	280	340	400	500	ps
Data hold skew factor	t_{QHS}	max		260	280	340	400	480	600	ps
DQS Output High Pulse Width	t_{QSH}	min		t_{CH}(abs) - 0.05						t_{CK}(avg)
DQS Output Low Pulse Width	t_{QSL}	min		t_{CL}(abs) - 0.05						t_{CK}(avg)
Data Half Period	t_{QHP}	min		min(t_{QSH}, t_{QSL})						t_{CK}(avg)
DQ/DQS output hold time from DQS	t_{QH}	min		t_{QHP}-t_{QHS}						ps
Read preamble	t_{RPRE}	min		0.9						t_{CK}(avg)
Read Postamble	t_{RPST}	min		t_{CL}(abs) - 0.05						t_{CK}(avg)
DQS low-Z from clock	$t_{LZ(DQS)}$	min		$t_{DQSCK(min)}$ - 300						ps
DQ low-Z from clock	$t_{LZ(DQ)}$	min		$t_{DQSCK(min)}$ - (1.4*$t_{QHS(max)}$)						ps
DQS high-Z from clock	$t_{HZ(DQS)}$	max		$t_{DQSCK(max)}$ - 100						ps

Parameter	Symbol	min/max	min t_{CK}	LPDDR2						Unit
				933	800	667	533	400	333	Mbps
Write Parameters										
DQ and DM input hold time (Vref based)	t_{DH}	min		235	270	350	430	480	600	ps
DQ and DM input setup time (Vref based)	t_{DS}	min		235	270	350	430	480	600	ps
DQ and DM input pulse width	t_{DIPW}	min		0.35						t_{CK}(avg)
Write command to 1st DQS latching transition	t_{DQSS}	min		0.75						t_{CK}(avg)
		max		1.25						t_{CK}(avg)
DQS input high-level width	t_{DQSH}	min		0.4						t_{CK}(avg)
DQS input low-level width	t_{DQSL}	min		0.4						t_{CK}(avg)
DQS falling edge to CK setup time	t_{DSS}	min		0.2						t_{CK}(avg)
DQS falling edge hold time from CK	t_{DSH}	min		0.2						t_{CK}(avg)
Write postamble	t_{WPST}	min		0.4						t_{CK}(avg)
Write preamble	t_{WPRE}	min		0.35						t_{CK}(avg)
CKE Input Parameters										
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3						t_{CK}(avg)
CKE input setup time	t_{ISCKE}	min		0.25						t_{CK}(avg)
CKE input hold time	t_{IHCKE}	min		0.25						t_{CK}(avg)
Command Address Input Parameters										
Address & control input setup time (Vref based)	t_{IS}	min		250	290	370	460	600	740	ps
Address & control input hold time (Vref based)	t_{IH}	min		250	290	370	460	600	740	ps
Address & control input pulse width	t_{IPW}	min		0.40						t_{CK}(avg)
Boot Parameters (10 MHz - 55 MHz)										
Clock Cycle Time	t_{CKb}	max	-	100						ns
		min		18						
CKE input setup time	t_{ISCKEb}	min	-	2.5						ns
CKE input hold time	t_{IHCKEb}	min	-	2.5						ns
Address & control input setup time	t_{ISb}	min	-	1150						ps
Address & control input hold time	t_{IHb}	min	-	1150						ps
DQS Output data access time from CK_t/CK_c	t_{DQSCKb}	min	-	2.0						ns
		max		10.0						
Data strobe edge to output data edge t_{DQSQb}-1.2	t_{DQSQb}	max	-	1.2						ns
Data hold skew factor	t_{QHSb}	max	-	1.2						ns
Mode Register Parameters										
Mode Register Write command period	t_{MRW}	min	5	5						t_{CK}(avg)
Mode Register Read command period	t_{MRR}	min	2	2						t_{CK}(avg)

Parameter	Symbol	min/max	min t_{CK}	LPDDR2						Unit
				933	800	667	533	400	333	Mbps
LPDDR2 SDRAM Core Parameters										
Read Latency	RL	min	3	7	6	5	4	3	3	t_{CK}(avg)
Write Latency	WL	min	1	4	3	2	2	1	1	t_{CK}(avg)
Active to Active command period	t_{RC}	min	-	t_{RAS} + t_{RPab} (with all-bank Precharge) t_{RAS} + t_{RPpb} (with per-bank Precharge)						ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15						ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	t_{RFCab}+10						ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5						ns
LPDDR2-S4 CAS to CAS delay	t_{CCD}	min	2	2						t_{CK}(avg)
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5						ns
RAS to CAS Delay	t_{RCD}	min	3	18						ns
Row Precharge Time (single bank)	t_{RPpb}	min	3	18						ns
Row Precharge Time (all banks)	t_{RPab}	min	3	21						ns
Row Active Time	t_{RAS}	min	3	42						ns
		max	-	70						µs
Write Recovery Time	t_{WR}	min	3	15						ns
Internal Write to Read command delay	t_{WTR}	min	2	7.5				10		ns
Active bank A to Active bank B	t_{RRD}	min	2	10						ns
Four Bank Activate window	t_{FAW}	min	8	50					60	ns
Minimum Deep Power Down time	t_{DPD}	min		500						µs

5 Block Diagram

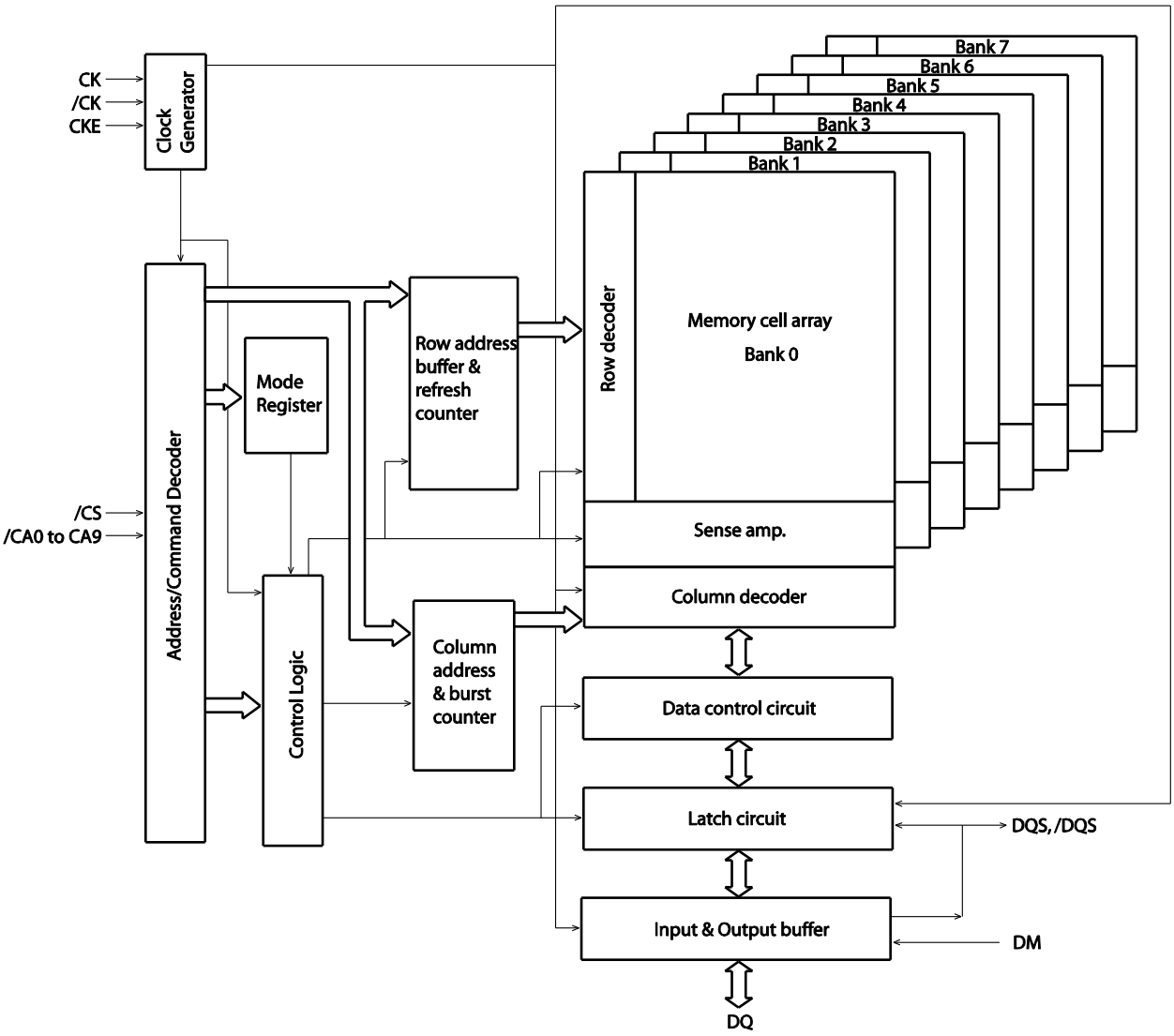


Figure 2. Block Diagram

6 Pin Function

6.1 CK, /CK (input pins)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When in a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When in a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK and the /CK. The other input signals are referred at CK rising edge.

6.2 /CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

6.3 CA0 to CA9 (input pins)

These pins define the row & column addresses and operating commands (read, write, etc.) depend on their voltage levels. See "Addressing Table" and “Command operation”.

6.4 [Addressing Table]

Page Size	Organization	Row address	Column address
2KB	x 16 bits	R0 to R13	C0[*1] to C9
	x 32 bits	R0 to R13	C0[*1] to C8

Command	DDR CA Pins										CK edge
	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
Active	--	--	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	R0	R1	R2	R3	R4	R5	R6	R7	R13	--	↓
Write/Read	--	--	--	--	--	C1	C2	BA0	BA1	BA2	↑
	AP	C3	C4	C5	C6	C7	C8	C9	--	--	↓

Remarks: Rx = row address. Cx = column address

Notes:
1) C0 is not present on the command & address, therefore C0 is implied to be zero.
2) BA0,1 &2 are bank select signals. The memory array is divided into banks 0, 1, 2, 3, 4, 5, 6 and 7. BA0, 1 & 2 define to which bank an active/read/write/precharge command is being applied.
3) AP defines the precharge mode when a read command or a write command is issued. If AP = high during a read or write command, auto precharge function is enabled.

6.5 [Bank Numbering and BA Input Table]

	BA0	BA1	BA2
Bank0	L	L	L
Bank1	H	L	L
Bank2	L	H	L
Bank3	H	H	L
Bank4	L	L	H
Bank5	H	L	H
Bank6	L	H	H
Bank7	H	H	H

Remarks: H = VIH, L = VIL.

6.6 CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least if CKE changes at the crossing point of the CK rising edge and the /CK falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

6.7 DQ0 to DQ15 (x16), DQ0 to DQ31 (x32) - (input/output pins)

Data are input to and output from these pins.

6.8 DQSx, /DQSx (input/ output pins, where x = 0 to 3)

DQS and /DQS provide the read data strobes (as output) and the write data strobes (as input). Each DQS (/DQS) pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

6.9 DM0 to DM3 (input pins)

DM is the reference signals of the data input mask function. DM is sampled at the crossing point of DQS and VDDQ/2. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up.

6.10 [DM truth table]

Name (Functional)	DM	DQ	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:
1) Used to mask write data. Provided coincident with the corresponding data.
2) Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

6.11 [DQS and DM Correspondence Table]

Part Number	Organization	DQS	Data Mask	DQ
AD220016D	x 16 bits	DQS0, /DQS0	DM0	DQ0 to DQ7
		DQS1, /DQS1	DM1	DQ8 to DQ15
AD220032D	x 32 bits	DQS0, /DQS0	DM0	DQ0 to DQ7
		DQS1, /DQS1	DM1	DQ8 to DQ15
		DQS2, /DQS2	DM2	DQ16 to DQ23
		DQS3, /DQS3	DM3	DQ24 to DQ31

6.12 VDD1, VSS, VSS2, VDDCA, VSSCA, VDDQ, VSSQ (power supply)

VDD1/2 and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers. VDDCA and VSSCA are power supply pins for command address input buffers.

7 Command Operation

7.1 Command Truth Table

The LPDDR2 RAM recognizes the following commands specified by the /CS, CA0, CA1, CA2, CA3 and CKE at the rising edge of the clock.
CAxr refers to the command/address bit x on the rising edge of clock. (↑)
CAxf refers to the command/address bit x on the falling edge of clock. (↓)

Function	Symbol	CKE		/CS	DDR CA Pins										CK edge
		Previous cycle	Current cycle		CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
Mode register write	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				×	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
Mode register read	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				×	MA6	MA7	×								↓
Refresh per bank	REFpb	H	H	L	L	L	H	L	×						↑
				×	×										↓
Refresh all banks	REFab	H	H	L	L	L	H	H	×						↑
				×	×										↓
Self-refresh entry	SELF	H	L	L	L	L	H	×							↑
		×		×	×										↓
Bank activate	ACT	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				×	R0	R1	R2	R3	R4	R5	R6	R7	R13	×	↓
Write	WRIT	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				×	AP[*1]	C3	C4	C5	C6	C7	C8	C9	×		↓
Read	READ	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				×	AP[*1]	C3	C4	C5	C6	C7	C8	C9	×		↓
Precharge	PRE	H	H	L	H	H	L	H	AB	×		BA0	BA1	BA2	↑
				×	×										↓
Burst terminate	BST	H	H	L	H	H	L	L	×						↑
				×	×										↓
Deep power-down mode entry	DPDEN	H	L	L	H	H	L	×							↑
		×		×	×										↓
No operation	NOP	H	H	L	H	H	H	×							↑
				×	×										↓
Maintain PD/SREF/DPD	NOP	L	L	L	H	H	H	×							↑
				×	×										↓
No operation	NOP	H	H	H	×										↑
				×	×										↓
Device deselect	DESL	H	H	H	×										↑
				×	×										↓
Power-down mode entry	PDEN	H	L	H	×										↑
		×		×	×										↓
Exit power-down/deep power-down mode, self refresh	PDEX, SELFX, DPDX	L	H	H	×										↑
		×		×	×										↓

Remarks: H = VIH, L = VIL, × = VIH or VIL, Rx = row address, Cx = column address,
AB = all banks or selected bank precharge.

Notes:

1) AP high during a read or write command indicates that an auto precharge will occur to the bank associated with the read or write command.
2) Bank selects (BA0, 1 & 2) determine which bank is to be operated upon.
3) Self-refresh exit and deep power-down exit are asynchronous.
4) /CS and CKE are sampled at the rising edge of clock.
5) VREF must be maintained during self-refresh and deep power-down operation.

7.2 Register Commands [MRR/MRW]

The register commands include both a mode register read (MRR) and a mode register write (MRW) command. The protocol provides support for a total of up to 256 8-bit registers, which will be either read-only, write-only, or both readable and writeable by the memory controller.

7.3 Refresh Commands [REF]

The refresh commands include an All Banks refresh command, and a self-refresh command. Entry into self-refresh mode will occur upon the transition of CKE from high to low.

7.4 Active Command [ACT]

Only CA0r and CA1r are needed to encode this command. The remaining bits in the CA map specify the row and bank address.

7.5 Read/Write Commands [READ/WRIT]

The read and write commands indicate whether a read or write is desired. CA0r, CA1r, and CA2r are needed to encode either command. The remaining bits in the CA map are used to indicate the column address. A bit to indicate whether an auto precharge is desired is provided and is registered on CA0f of both read and write commands. Two bits in the read and write command encoding have been specified as Reserved for Future Use (RFU).

7.6 Precharge Commands [PRE]

The Precharge command requires that the bank be specified at command time only when the auto precharge bit indicates that an All Bank pre-charge is not desired (I.E. AB (CA4r) = 0). If the All Bank precharge bit is set (I.E. AB (CA4r) = 1), bank information is not required.

7.7 Burst Terminate Command [BST]

The BST command will allow for both read and write commands (without auto precharge) to be interrupted on prefetch boundaries prior to the end of a burst. The desired burst length will be set in one of the mode registers.

7.8 Power-down and Deep Power Down [PDEN/DPDEN]

Both power-down and deep power-down modes are supported by the protocol. In normal power-down mode all input and output buffers as well as CK and /CK will be disabled. If all banks are precharged prior to entering power-down mode, the device will be said to be in Precharge power-down mode. If at least one bank is open while entering power-down mode, the SDRAM device will be said to be in Active power-down mode.
In Deep power-down mode all input/output buffers, CK, /CK, and power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode.
The command for entry into normal power-down mode requires that /CS is high, while the command for entry into Deep power-down mode requires that /CS be low. In both cases CKE will remain active and will be the mechanism by which the SDRAM is able to exit either power-down modes.

7.9 Exit Command [PDEX, DPDX, SELFX]

Exit from self-refresh, power down, or deep power-down modes requires a low to high transition of CKE.

7.10 No Operation Command [NOP]

NOP can either be issued using a command when /CS is low or by simply deselecting /CS.

7.11 CKE Truth Table

	CKE		Command (n)*3		
Current state*2	Previous cycle (n-1)*1	Current cycle (n)*1	/CS, CA0r to CA3r	Operation (n)*3	Notes
Active/Idle power-down	L	L	×	Maintain power-down	8
	L	H	DESL or NOP	Power-down exit	4
Deep power-down entry	L	L	×	Maintain power-down	8
	L	H	DESL or NOP	Deep power-down exit	
Self-refresh	L	L	×	Maintain self-refresh	8
	L	H	DESL or NOP	Self-refresh exit	4, 7
Bank Active	H	L	DESL or NOP	Active power down entry	4
All banks idle	H	L	DESL or NOP	Precharge power down entry	4
	H	L	SELF	Self-refresh entry	5
Other	H	H	Refer to the Command Truth Table		6

Remark: H = VIH, L = VIL, × = Don't care

Notes:

1) CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
2) Current state is the state of the LPDDR2 RAM immediately prior to clock edge n.
3) Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n).
4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5) Self-refresh mode can only be entered from the all banks idle state.
6) Must be a legal command as defined in the command truth table.
7) Valid commands for deep power-down exit and power-down exit and self-refresh exit are NOP and DESL only.
8) Deep power-down, power-down and self-refresh cannot be entered while read/write operations, mode register read/write or precharge operations are in progress.
9) VREF must be maintained during self-refresh operation.
10) Clock frequency may be changed or stopped during the active power-down or idle power-down state.

8 Simplified State Diagram

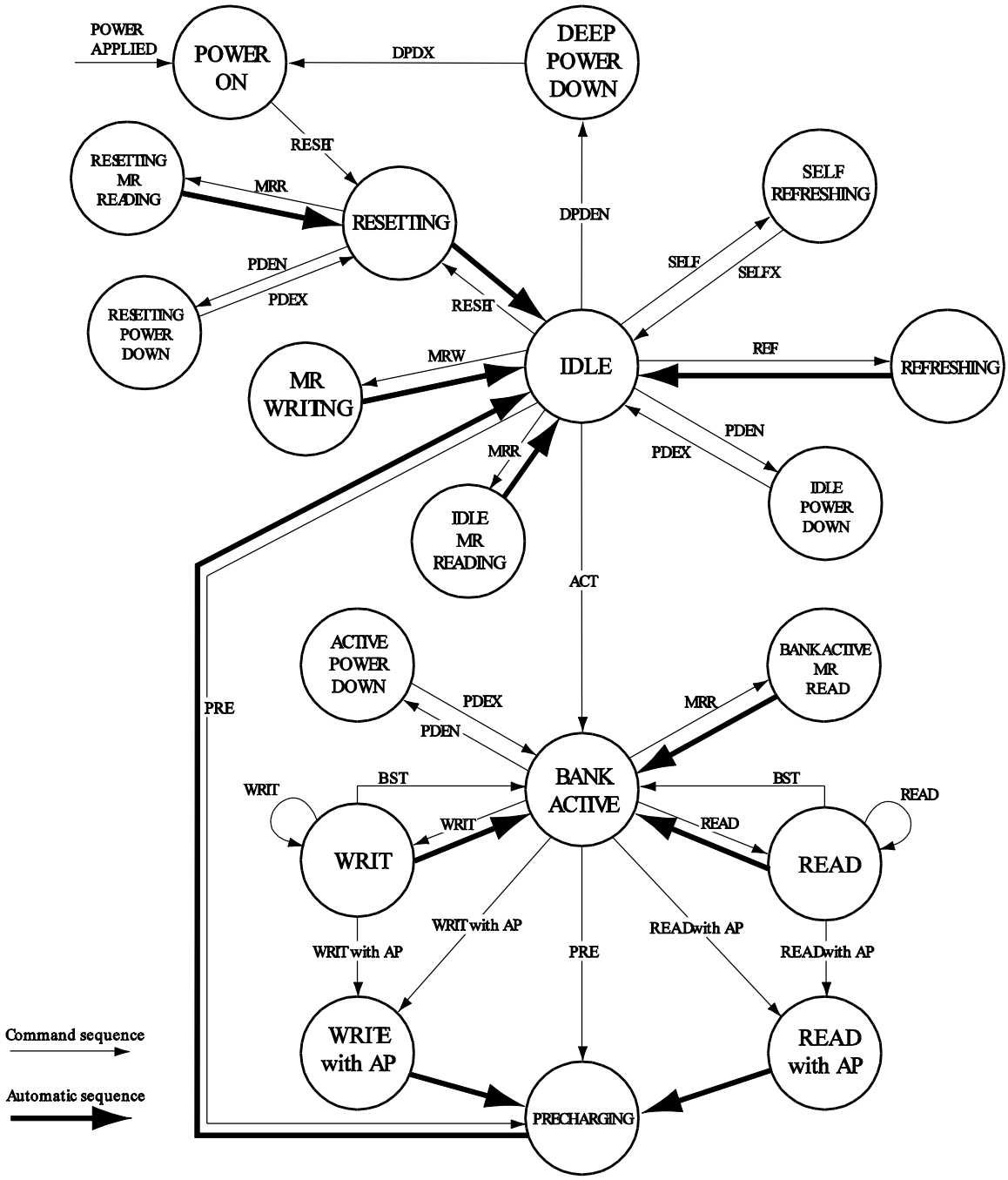


Figure 3 Simplified State Diagram

9 Operation of the LPDDR2 RAM

Read and write accesses to the LPDDR2 RAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four, eight, and sixteen in a programmed sequence. Accesses begin with the registration of an active command, which is then followed by a read or write command. The address bits registered coincident with the active command is used to select the bank and row to be accessed (BA0,1 & 2 selects the bank; R0 to R13 selects the row). The address bits registered coincident with the read or write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operations, the LPDDR2 RAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

9.1 LPDDR2 RAM Power-On and Initialization Sequence

9.1.1 Power Ramp and Device Initialization

Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (≤0.2 × VDDCA), all other inputs shall be between VIL (min.) and VIH (max.). The LPDDR2 RAM device will only guarantee that outputs are in a high impedance state while CKE is held low. On or before the completion of the power ramp (Tb) CKE must be held low. Voltage levels at I/Os and outputs must be between VSSQ and VDDQ during voltage ramp time to avoid latch-up.

The following conditions apply:

- Ta is the point where any power supply first reaches 300mV.
- After Ta is reached, VDD1 must be greater than VDD2 – 200mV.
- After Ta is reached, VDD1 and VDD2 must be greater than VDDCA – 200mV.
- After Ta is reached, VDD1 and VDD2 must be greater than VDDQ – 200mV.
- After Ta is reached, VREF must always be less than all other supply voltages.
- The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.
- Tb is the point when all supply and reference voltages are within their respective min/max operating conditions.
- Power ramp duration tINIT0 (Tb – Ta) must be no greater than 20ms.

Note: VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

CKE and Clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100ns, after which it may be asserted high. Clock must be stable at least tINIT2 = 5tCK prior to the first low to high transition of CKE (Tc). CKE, /CS and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

Reset Command

After tINIT3 is satisfied, a MRW (Reset) command shall be issued (Td). Wait for at least tINIT4 = 1µs while keeping CKE asserted and issuing NOP or DESL commands.

Mode Register Reads and Device Auto-Initialization (DAI) polling

After tINIT4 is satisfied (Te), only MRR commands (including power-down entry/exit) are allowed. It is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0, Device ID, etc.). The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete. As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured. After the DAI-bit (MR0.DAI) is set to "ready" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0 DAI. The LPDDR2 RAM will set the DAI-bit no later than tINIT5 (10µs) after the Reset command.

Normal Operation

After tINIT5 (Tf), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. The LPDDR2 RAM device will now be in IDLE state and ready for any valid command. After Tf, the clock frequency may be changed according to the clock frequency change procedure described in section Input Clock Stop and Frequency Change during Power-Down of this specification.

9.1.2 Timing Parameters for Initialization

Symbol	Value		Unit	Test Condition
	min.	max.		
tINIT0	--	20	ms	Maximum Power Ramp Time
tINIT1	100	--	ns	Minimum CKE low time after completion of power ramp
tINIT2	5	--	tCK	Minimum stable clock before first CKE high
tINIT3	200	--	µs	Minimum Idle time after first CKE assertion
tINIT4	1	--	µs	Minimum Idle time after Reset command, this time will be about 2 × tRFCab (max density) + tRP
tINIT5	--	10	µs	Maximum duration of Device Auto-Initialization
tCKBOOT	18	100	ns	Clock cycle time during boot

[See Figure 134 in JEDEC Standard No. 209-2E]

Initialization After RESET (without power ramp)

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-off Sequence

The following procedure is required to power off the device.
While powering off, CKE must be held LOW (≤0.2 × VDD2);.all other inputs must be between VILmin and VIHmax.
The device outputs remain at High-Z while CKE is held LOW.
DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up.
CK_t, CK_c, CS_n, and CA input levels must be between VSS and VDD2 during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see the following Table).

Between…	*Applicable Conditions*
Tx and Tz	V_{DD1} must be greater than V_{DD2} -- 200mV
Tx and Tz	V_{DD1} must be greater than V_{DDCA} -- 200mV
Tx and Tz	V_{DD1} must be greater than V_{DDQ} -- 200mV
Tx and Tz	V_{REF} must always be less than all other supply voltages

The voltage difference between any of VSS and VSSQ pins must not exceed 100mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:
At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

Power-up, Initialization, and Power-off (cont'd)

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Symbol	*Value*		*Unit*	*Comment*
	min.	*max.*		
t_{POFF}	--	2	s	Maximum Power-Off ramp time

9.2 Programming the Mode Register

9.2.1 Mode Register Assignment

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Remark
0	00h	Device Info.	R	(RFU)						DI	DAI	See MR0
1	01h	Device Feature 1	W	nWR (for AP)			WC	BT	BL			See MR1
2	02h	Device Feature 2	W	(RFU)				RL & WL				See MR2
3	03h	I/O Config-1	W	(RFU)				DS				See MR3
4	04h	SDRAM Refresh Rate	R	TUF	(RFU)				Refresh Rate			See MR4
5	05h	Basic Config-1	R	Company ID								See MR5
6	06h	Basic Config-2	R	Revision ID1								See MR6
7	07h	Basic Config-3	R	Revision ID2								See MR7
8	08h	Basic Config -4	R	I/O Width		Density				Type		See MR8
9	09h	Test Mode	W*[1]	Vendor-Specific Test Mode								See MR9
10	0Ah	IO Calibration	W	Calibration Code								See MR10
11:15	0Bh TO 0Fh	Reserved		(RFU)								
16	10h	PASR_Bank	W	Bank Mask								See MR16
17	11h	PASR_Seg	W	Segment Mask								See MR17
18:23	12h TO 17h	Reserved		(RFU)								

MR No.24 to 31 are Non-Volatile Memory (NVM) specific mode registers, which LPDDR2 does not have.

32	20h	Calibration Pattern A	R	Calibration Pattern A	See MR32
40	28h	Calibration Pattern B	R	Calibration Pattern B	See MR40
63	3FH	Reset	W	×	See MR63

MR No. 33 to 39, 41 to 62 and MR 64 to 255 are reserved.

Note: MR9[5] is Fail Bit, and Read-Only.

Remarks: R = read-only , W = write-only
DAI = Device Auto-Initialization
DI = Device Information
nWR = Write Recovery for auto precharge
WC = Wrap Control
BT = Burst Type
BL = Burst Length
RL & WL = Read latency & Write latency
DS = Drive Strength
TUF = Temperature Update Flag

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	(RFU)						DI	DAI

Device Auto-Initialization	Read-only	0	DAI complete
		1	DAI still in progress
Device Information	Read-only	0	SDRAM
		1	Reserved

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR1	nWR (for AP)			WC	BT	BT		

Burst Length	Write-only	010	BL4 (default)
		011	BL8
		100	BL16
		Other	Reserved
Burst Type	Write-only	0	Sequential (default)
		1	Interleaved
Wrap Control	Write-only	0	Wrap (default)
		1	No Wrap
Write Recovery for Autoprecharge*	Write-only	001	nWR=3 (default)
		010	nWR=4
		011	nWR=5
		100	nWR=6
		101	nWR=7
		110	nWR=8
		Other	Reserved

Note: Programmed value in nWR register is the number of clock cycles which determined when to start internal precharge operation for a write burst with AP enabled. It is determined by RU (tWR/tCK).

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR2	(RFU)				RL & WL			

Read latency and Write latency	Write-only	0001	RL3/WL1 (default)
		0010	RL4/WL2
		0011	RL5/WL2
		0100	RL6/WL3
		0101	RL7/WL4
		0110	RL8/WL4
		Other	Reserved

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR3	(RFU)				DS			

Drive Strength	Write-only	0000	Reserved
		0001	34.3Ω typical
		0010	40Ω typical (default)
		0011	48Ω typical
		0100	60Ω typical
		0101	reserved for 68.6Ω typical
		0110	80Ω typical
		0111	120Ω typical
		Other	Reserved

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR4	TUF	(RFU)				Refresh Rate		

Refresh Rate	Read-only	000	Reserved
		001	Reserved
		010	2 × tREFI
		011	1 × tREFI
		100	Reserved
		101	0.25 × tREFI, set to 85C, do not derate
		110	0.25 × tREFI, set to 95C, de-rate
		111	temp>105C, set to 105C, stall
Temperature Update Flag	Read-only	0	OP<2:0> value has not changed since last read of MR4.
		1	OP<2:0> value has changed since last read of MR4.

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR5	Company ID							

Company ID	Read-only	11111101	AP Memory

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR6	Revision ID1							

Revision ID1	Read-only	00000000	Version A

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR7	Revision ID2							

Revision ID2	Read-only	00000000	Version A

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR8	I/O Width		Density				Type	

Type	Read-only	**00**	**S4 SDRAM**
		01	Reserved
		10	Reserved
		11	Reserved
Density	Read-only	0010	256Mb
		0011	512Mb
		0100	1Gb
		0101	**2Gb**
		0110	4Gb
		0111	8Gb
		1000	16Gb
		1001	32Gb
		Other	Reserved
I/O Width	Read-only	00	x32
		01	x16
		10	x8
		11	Not used

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR9	Vendor-Specific Test Mode							

Failed Die Bit[5]	Read-only	0	Pass (default)
		1	Fail
Tested Die Bit [4]	Read-only	0	Reserved
		1	Reserved

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR10	Calibration Code							

Calibration Code	Write-only	hFF	Calibration command after initialization
		hAB	Long calibration
		h56	Short calibration
		hC3	ZQ Reset
		others	Reserved

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR16	Bank Mask							

Bank [7:0] Mask	Write-only	0	Refresh enable to the bank (=unmasked, default)
		1	Refresh blocked (=masked)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR17	Segment Mask							

Seg [7:0] Mask	Write-only	0	Refresh enable to the segment (=unmasked, default)
		1	Refresh blocked (=masked)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR32	Calibration Pattern "A"							

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
DQ outputs pattern A	1	0	1	0

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR40	Calibration Pattern "B"							

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
DQ outputs pattern B	0	0	1	1

9.3 Bank Activate Command [ACT]

The bank activate command is issued by holding /CS low, CA0 low, and CA1 high at the rising edge of the clock. The bank addresses BA0, 1 & 2 are used to select the desired bank. The row address R0 through R13 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any read or write operation can be executed. Immediately after the Bank Active command, the LPDDR2 RAM can accept a read or write command on the following clock cycle at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another bank activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive bank activate commands to the same bank is determined by the /RAS cycle time of the device (tRC). The minimum time interval between successive bank activate commands to the different bank is determined by (tRRD).

[See Figure 19 in JEDEC Standard No. 209-2E]

9.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /CS low, CA0 high, and CA1 low at the rising edge of the clock. CA2r must also be defined at this time to determine whether the access cycle is a read operation (CA2r high) or a write operation (CA2r low).

The LPDDR2 RAM provides a fast column access operation. A single read or write command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 8M bits x 16 I/O x 8 banks chip has a page length of 16384 bits (defined by C1 to C11). The page length of 16384 is divided into 4096, 2048, or 1024 for 16 bits burst respectively. A 4 bits or 8 bits or 16 bits burst operation will occur entirely within one of the 4096, 2048, or 1024 groups beginning with the column address supplied to the device during the read or write command (C1 to C11). The second, third and fourth access will also occur within this group segment. However, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bits burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, reads may be interrupted by reads and writes may be interrupted by writes provided that this occurs on a 4 bits boundary. The minimum CAS to CAS delay is defined by tCCD.

9.5 Burst Mode Operation

							Burst cycle number and burst address sequence															
C3 (CA1f)	C2 (CA6r)	C1 (CA5r)	C0 (0)	BL	BT	WC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
×	×	0	0	4	any	Wrap	0	1	2	3												
×	×	1	0				2	3	0	1												
×	×	×	0		any	NW*5	y	y+1	y+2	y+3												
×	0	0	0	8	Seq	Wrap	0	1	2	3	4	5	6	7								
×	0	1	0				2	3	4	5	6	7	0	1								
×	1	0	0				4	5	6	7	0	1	2	3								
×	1	1	0				6	7	0	1	2	3	4	5								
×	0	0	0		Int		0	1	2	3	4	5	6	7								
×	0	1	0				2	3	0	1	6	7	4	5								
×	1	0	0				4	5	6	7	0	1	2	3								
×	1	1	0				6	7	4	5	2	3	0	1								
0	0	0	0	16	Seq	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	0				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0	1	0	0				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0	1	1	0				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1	0	0	0				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1	0	1	0				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1	1	0	0				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1	1	1	0				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D

Remarks: NW: no wrap. Int: interleaved. Seq: sequential. Any: sequential or interleaved.
C3 = CA1f. C2 = CA6r. C1 = Ca5r. C0=0.
Notes:
C0 input is not present on CA bus. It is implied zero.
For BL = 4, the burst address represents C1 to C0.
For BL = 8, the burst address represents C2 to C0.
For BL = 16, the burst address represents C3 to C0.
Non-wrap, BL4, data-orders shown below are prohibited:
Not across full page boundary. (x16: 3FE, 3FF, 000, 001)
(x32: 1FE, 1FF, 000, 001)
Not across sub page boundary. (x16: 1FE, 1FF, 200, 201)

9.6 Burst Read Command [READ]

The Burst Read command is initiated by having /CS low, CA0 high, CA1 high and CA2 low at the rising edge of the clock. The address inputs, CA5r to CA4r and CA1f to CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the read command is issued to the rising edge of the clock from which the

tDQSCK delay is measured. The first valid datum is available RL + tDQSCK + tDQSQ after the rising edge of the clock where the read command is issued. The data strobe output (DQS) is driven low tRPRE before valid data (DQ) is driven onto the data bus.

The first bit of the burst is synchronized with the first rising edge of the data strobe (DQS). Each subsequent dataout appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is defined by mode register.

Pin timings are measured relative to the cross point of DQS and its complement, /DQS.

[See Figures 24, 25 in JEDEC Standard No. 209-2E]

[See Figure 33 in JEDEC Standard No. 209-2E]

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU (tDQSCKmax/tCK) + BL/2 + 1 – WL. Note that if a read burst is interrupted with a Burst Terminate (BST) command, the effective BL of the interrupted read burst should be used to calculate the minimum read to write latency.

[See Figure 35 in JEDEC Standard No. 209-2E]

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 16 clocks for BL = 16 operation. This operation is allowed regardless of whether the same or different banks as long as the banks are activated.

Burst read can only be interrupted by another read with 4 bits burst boundary.

[See Figure 37 in JEDEC Standard No. 209-2E]

Notes:
Read burst interrupt function is only allowed on burst of 8 and 16.
Read burst interrupt may only occur on even clocks after the previous read commands provided that tCCD is met.
Reads can only be interrupted by other reads or the BST command.
Read burst interruption is allowed to any bank inside SDRAM.
Read burst with auto precharge is not allowed to be interrupted.
The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

9.7 Burst Write Command [WRIT]

The Burst Write command is initiated by having /CS low, CA0 high, CA1 high and CA2 high at the rising edge of the clock. The address inputs determine the starting column address. The first valid datum is available Write Latency (WL) cycles + tDQSS from the rising edge of the clock from which the Write command is driven. A data strobe signal (DQS) should be driven low (preamble) nominally half clock prior to the data input. The first data bit of the burst cycle must be applied to the DQ pins tDS prior to the first rising edge of the DQS following the preamble. The subsequent burst bit data are sampled on successive edges of the DQS until the burst length is completed, which is 4, 8 or 16 bit burst.

tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation. Pin timings are measured relative to the crossing point of DQS and its complement, /DQS.

[See Figure 42 in JEDEC Standard No. 209-2E]

[See Figure 45 in JEDEC Standard No. 209-2E]

The minimum number of clocks from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU (tWTR/tCK)]. If a write burst is interrupted with a Burst Terminate (BST) command, the effective BL of the interrupted write burst should be used to calculate the minimum write to read latency.

[See Figure 47 in JEDEC Standard No. 209-2E]

The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Burst write can only be interrupted by another write with 4 bits burst boundary, provided that tCCD is met.

[See Figure 49 in JEDEC Standard No. 209-2E]

Notes:
Write burst interrupt function is only allowed on burst of 8 and 16.
Write burst interrupt may only occur on even clocks after the previous write commands, provided that tCCD is met.
Writes can only be interrupted by other writes or the BST command.
Write burst interruption is allowed to any bank inside SDRAM.
Write burst with auto precharge is not allowed to be interrupted.

9.8 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on LPDDR2 RAM.
DM can mask input data. By setting DM to low, data can be written. When DM is set to high, the corresponding data is not written, and the previous data is held.

The latency between DM input and enabling/disabling mask function is 0.

[See Figure 57 in JEDEC Standard No. 209-2E]

9.9 Precharge Command [PRE]

The precharge command is used to precharge or close a bank that has been activated. The precharge command is initiated by having /CS low, CA0 high, CA1 high, CA2 low, and CA3 high at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. Three address bits CA4r, CA7r and CA8r are used to define which bank to precharge when the command is issued.

CA4r	CA7r	CA8r	CA9r	Precharged bank(s)
L	L	L	L	Bank 0 only
L	H	L	L	Bank 1 only
L	L	H	L	Bank 2 only
L	H	H	L	Bank 3 only
L	L	L	H	Bank 4 only
L	H	L	H	Bank 5 only
L	L	H	H	Bank 6 only
L	H	H	H	Bank 7 only
H	×	×	×	All banks

Remark: H = VIH, L = VIL, × = VIH or VIL

9.10 Burst Read Operation Followed by Precharge

For the earliest possible precharge, the precharge command may be issued on the rising edge of clock BL/2 clocks after a read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.

The minimum read to precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefretch of a read to precharge command. This time is called tRTP (Read to Precharge).

[See Figure 64 in JEDEC Standard No. 209-2E]

9.11 Burst Write Operation Followed by Precharge

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the precharge command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No precharge command should be issued prior to the tWR delay. Minimum Write to Precharge command spacing to the same bank is WL + BL/2 + RU (tWR/tCK) clock cycles. If the data burst is interrupted with a BST command, the effective BL shall be used to calculate the minimum Write to Precharge spacing.

[See Figure 67 in JEDEC Standard No. 209-2E]

9.12 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the LPDDR2 RAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If AP is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If AP is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge on the rising edge which is Read Latency (RL) clock cycles before the end of the read burst.

Auto precharge can also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read latency) thus improving system performance for random data access.

9.13 Burst Read with Auto Precharge

If AP (CA0f) is high when a read command is issued, the read with auto precharge function is engaged. The LPDDR2 RAM starts an auto precharge operation on the rising edge of the clock BL/2 or RU (tRTP/tCK) cycles later than the read with AP command.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

The /RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

[See Figure 68 in JEDEC Standard No. 209-2E]

9.14 Burst Write with Auto Precharge

If AP (CA0f) is high when a write command is issued, the write with auto precharge function is engaged. The LPDDR2 RAM starts with an auto precharge operation on the rising edge of which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

The data-in to bank activate delay time (tWR + tRP) has been satisfied.
The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

[See Figure 70 in JEDEC Standard No. 209-2E]

The LPDDR2 RAM supports the concurrent auto precharge feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any column command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply. (E.G. Conflict between READ data and WRITE data must be avoided.)

The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below.

From command	To command (different bank, non-interrupting command)	Minimum delay (concurrent AP supported)	Units
Read w/ AP	Read or Read w/ AP	BL/2	tCK
	Write or Write w/ AP	(BL/2) + 2	tCK
	Precharge or Activate	1	tCK
Write w/ AP	Read or Read w/ AP	WL + (BL/2) + tWTR	tCK
	Write or Write w/ AP	BL/2	tCK
	Precharge or Activate	1	tCK

The minimum delay from the read, write and precharge command to the precharge command to the same bank is summarized below.

From Command	To Command	Minimum delay between "From Command" to "To Command"	Units	Notes
Read	Precharge (to same bank as Read)	(BL/2) + Max (2, RU (tRTP/tCK)) -2	tCK	1
	Precharge all	(BL/2) + Max (2, RU (tRTP/tCK)) -2	tCK	1
Read w/ AP	Precharge (to same bank as Read w/ AP)	(BL/2) + Max (2, RU (tRTP/tCK)) -2	tCK	1
	Precharge all	(BL/2) + Max (2, RU (tRTP/tCK)) -2	tCK	1
Write	Precharge (to same bank as Write)	WL + (BL/2) + tWTR	tCK	1
	Precharge all	WL + (BL/2) + tWTR	tCK	1
Write w/ AP	Precharge (to same bank as Write w/ AP)	WL + (BL/2) + tWTR	tCK	1
	Precharge all	WL + (BL/2) + tWTR	tCK	1
Precharge	Precharge (to same bank as precharge)	1	tCK	1
	Precharge all	1	tCK	1
Precharge All	Precharge	1	tCK	1
	Precharge all	1	tCK	1

Notes:
For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.

9.15 The Burst Terminate [BST]

The Burst Terminate (BST) command is initiated by having /CS low, CA0 high, CA1 high, CA2 low, and CA3 low at the rising edge of clock. The 4-bit prefetch architecture allows the BST command to be asserted on an even number of clock cycles after a write or read command. The BST command only affects the most recent read or write command. The latency of the BST command following a read command is equal to the Read Latency (RL). The latency of the BST command following a Write command is equal to the Write Latency (WL). Therefore, the effective burst length of a Read or Write command interrupted by a BST command is an integer multiple of 4 and is defined as follows:

Effective BL = 2 × {Number of clocks from the read or write command to the BST command}

[See Figure 54 in JEDEC Standard No. 209-2E]

Burst Terminate interrupts the burst RL cycles after the BST command for reads. BST can only be issued an even number of clocks after the read command.

[See Figure 53 in JEDEC Standard No. 209-2E]

Burst Terminate interrupts the burst WL cycles after the BST command for writes. BST can only be issued an even number of clocks after the write command.

9.16 Refresh Command [REF]

The Refresh command is initiated by having /CS low, CA0 low, CA1 low, and CA2 high at the rising edge of clock. All Bank Refresh is initiated by having CA3 high at the rising edge of clock.

For All Bank Refresh, all banks of the LPDDR2 RAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started. When the All Bank refresh cycle has completed, all banks of the LPDDR2 RAM will be in the precharged (idle) state. A delay between the Refresh Command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given LPDDR2 RAM SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 × tREFI.

[See Figures 76, 77 in JEDEC Standard No. 209-2E]

9.17 Self-Refresh [SELF]

The self-refresh command can be used to retain data in the LPDDR2 RAM, even if the rest of the system is powered down. When in the self-refresh mode, the LPDDR2 RAM retains data without external clocking. The LPDDR2 RAM device has a built-in timer to accommodate self-refresh operation. The self-refresh command is defined by having CKE low, /CS low, CA0 low, CA1 low, and CA2 high at the rising edge of the clock. CKE must be high during the previous clock cycle. Once the command is registered, CKE must be held low to keep the device in self-refresh model. Once the LPDDR2 RAM has entered self refresh mode, all of the external signals except CKE, are “don’t care”. For proper self-refresh operation, all power supply pins (VDD1, VDD2, VDDQ and VREF) must be at valid levels. The SDRAM initiates a minimum of one refresh command internally within tCKE period once it enters self-refresh mode. The clock is internally disabled during self-refresh operation to save power. The minimum time that the LPDDR2 RAM must remain in self-refresh mode is tCKE. The user may change the external clock frequency or halt the external clock one clock after self-refresh entry is registered; however, the clock must be restarted and stable before the device can exit self-refresh operation.

The use of self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the LPDDR2 RAM requires a minimum of one extra auto refresh command before it is put back into self-refresh mode.

[See Figure 78 in JEDEC Standard No. 209-2E]

Note: Device must be in the “All banks idle” state prior to entering self refresh mode.

9.18 Mode Register Read Command

The mode register read command is used to read configuration and status data from mode registers. The mode register read (MRR) command is initiated by having /CS low, CA0 low, CA1 low, CA2 low, and CA3 high at the rising edge of the clock. The mode register is selected by {CA1f to CA0f, CA9r to CA4r}. The mode register contents are available on the first data beat of DQ0 to DQ7, RL + tDQSCK + tDQSQ after the rising edge of the clock where the mode register read command is issued. Subsequent data beats contain valid, but undefined content. The MRR command has a burst length of four. The MRR command may not be interrupted by the BST command, MRR command or any other read command. The MRR command period (tMRR) is 2 clocks.

[See Figure 79 in JEDEC Standard No. 209-2E]

Notes:
Mode register read has a burst length of four.

Mode register read may not be interrupted by subsequent read, MRR, or BST command.
Mode register data is valid only on DQ0 to DQ7 on the first beat. Subsequent beats contain valid, but undefined data.
The mode register read command period (tMRR) is 2 clocks. No command (other than NOP or DESL) is allowed during this period.

9.19 Mode Register Write Command

The mode register write command is used to write configuration data to mode registers. The mode register write (MRW) command is initiated by having /CS low, CA0 low, CA1 low, CA2 low, and CA3 low at the rising edge of the clock. The mode register is selected by {CA1f to CA0f, CA9r to CA4r}. The data to be written to the mode register is contained in CA9f to CA3f. The MRW command period is defined by tMRW.

The MRW may only be issued when all banks are in the idle pre-charge state or to issue a reset command.

The MRW command is also used to initiate the reset command. The reset command is allowed in both the Idle and row active states as well as the power on Initialization sequence and brings the device to the tRESET (tINIT4) state in the power on Initialization sequence.

[[See Figure 84 in JEDEC Standard No. 209-2E]

Note: The mode register write command period (tMRW) is 5 clocks. No command (other than NOP or DESL) is allowed during this period.

9.20 Power-Down [PDEN]

Power-down is synchronously entered when CKE is registered low and /CS high at the rising edge of clock. CKE is not allowed to go low while mode register read or write operations are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto precharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power-down.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, /CK and CKE. In power-down mode, CKE low must be maintained at the inputs should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Maximum power-down duration is limited by the refresh requirements of the device, which allows a maximum of 9 tREFI if maximum posting of REF is utilized immediately before entering power-down.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or deselect command). CKE high must be maintained until tCKE has been satisfied.

[See Figure 91 in JEDEC Standard No. 209-2E]

The pattern shown below can repeat over a long period of time. With this pattern, LPDDR2 RAM guarantees all AC and DC timing, voltage specifications with temperature and voltage drift.

[See Figure 93 in JEDEC Standard No. 209-2E]

[See Figure 95 in JEDEC Standard No. 209-2E]

[See Figure 96 in JEDEC Standard No. 209-2E]

[See Figure 97 in JEDEC Standard No. 209-2E]

[See Figure 99 in JEDEC Standard No. 209-2E]

[See Figure 100 in JEDEC Standard No. 209-2E]

[See Figure 101 in JEDEC Standard No. 209-2E]

[See Figure 102 in JEDEC Standard No. 209-2E]

[[See Figure 103 in JEDEC Standard No. 209-2E]

[See Figure 104 in JEDEC Standard No. 209-2E]

9.21 Deep Power-Down [DPDEN]

Deep power-down is synchronously entered when CKE is registered low with /CS low, CA0 high, CA1 high, and CA2 low at the rising edge of clock. In deep power-down mode, all input buffers except CKE, all output buffers, and the power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode.

The deep power-down state is asynchronously exited when CKE is registered high with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

[See Figure 105 in JEDEC Standard No. 209-2E]

9.22 Input Clock Stop and Frequency Change during Power-Down

LPDDR2 RAM input clock frequency can be changed under following conditions:
LPDDR2 RAM is in power down mode.
CKE must be at logic low level.
A minimum of 2 clocks must be waited after CKE goes low before clock frequency may change

In order to reduce power, the input clock may be stopped during power down. When exiting power down, the clock must be stable prior to CKE going high.

SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, CKE must be held at stable low levels. Once input clock frequency is changed, stable new clocks must be provided to SDRAM before precharge power down may be exited. Depending on new clock frequency an additional MRW command may need to be issued to appropriately set the WR, RL and so on.

[See Figure 91 in JEDEC Standard No. 209-2E]

9.23 Clock Stop

Stopping the clocks during idle periods is an effective way of reducing power consumption. In addition to clock stop during power-down states, LPDDR2 RAM also supports clock stop under the following conditions:
The last command (activate, read, write, precharge, mode register write, mode register read, refresh) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency.
The related timing conditions (tRCD, tWR, tRP, tMRR, tMRW, etc.) have been met.
CKE is held high.

When the above conditions have been met, the device is either in "idle state" or "row active" state and clock stop mode may be entered with CK held low and /CK held high.

Clock stop mode is exited by restarting the clock. At least one NOP command must be issued before the next command may be applied. Additional clock pulses might be required depending on the system characteristics.

[See Figure 91 in JEDEC Standard No. 209-2E]

9.24 No Operation Command [NOP]

The no operation command (NOP) should be used in cases when the LPDDR2 RAM is in an idle or a wait state. The purpose of the no operation command is to prevent the LPDDR2 RAM from registering any unwanted commands between operations. NOP command is holding /CS low, CA0 high, CA1 high, and CA2 high at the rising edge of the clock. NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

9.25 Deselect Command [DESL]

The deselect command (DESL) performs the same function as a no operation command. DESL command occurs when /CS is brought high at the rising edge of the clock.

Change History			
Rev. #	Who	When	What
0.0	Conan	2014-05-22	Initial Version
0.1	Conan	2015-02-05	part# change, tRPab, added 2x tREFI
0.2	Conan	2015-05-13	added x16 part#, correction to package size & ball size
0.3	Conan	2015-06-10	updated current numbers from silicon, IDD6 to Typical + notes, removed notes from 2.5
0.4	Conan	2015-06-24	removed IDD4RQ
0.5	Conan	2015-09-04	updated IDD4R #
1.0	HCLIN	2015-11-18	updated operation temperature down to -40°C
1.1	HCLIN	2016-07-06	Corrected typo of interface & refresh requirement
1.2	HCLIN	2016-12-12	Corrected IDD4W spec
1.3	HCLIN	2017-03-10	Added package detail.
1.4	HCLIN	2017-08-10	Revised 134b package to 10x11.5(AB)
1.5	HCLIN	2017-12-20	Added 162b package of 8x10.5(ED)
1.6	Jecy	2017-12-22	Added 134b, 168b package
1.7	HCLIN	2018-04-15	Updated Pin Configuration of 134b of 1CS
1.8	Lance	2018-07-06	modify temperature grade code of PN from XT to X
1.9	Lance	2018-07-31	modify BGA134 ball assignment
2.0	Jerry	2019-03-29	updated IDD4R #
2.0a	David	2019-09-11	updated and reserved KGD datasheet for x16 and x32
2.1a	David	2019-11-14	Max CLK=466MHz with 134B -AB under normal range
2.1b	Jacky	2020-04-27	1.Modify MR4's access of Mode Register Assignment from W to R. 2.Modify bit[4] tested Die of MR9 to Reserved.
2.1c	Jacky	2020-05-13	1.Added Power-off Sequence description.